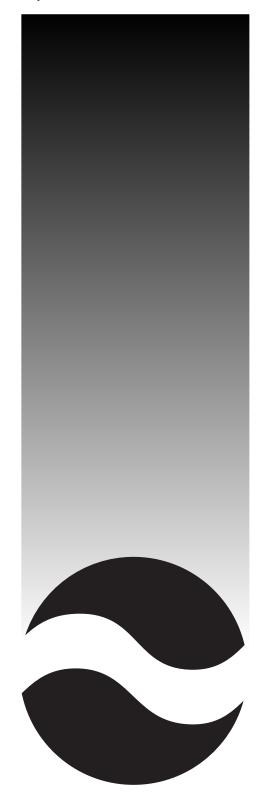
Supersedes Revision C March 2000

# JOINT INDUSTRY STANDARD

Requirements for Soldered Electrical and Electronic Assemblies





#### The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee (TAEC) adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

#### **Standards Should:**

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- · Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

#### **Standards Should Not:**

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

#### **Notice**

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

IPC Position Statement on Specification Revision Change It is the position of IPC's Technical Activities Executive Committee that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC publication is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision.

Adopted October 6, 1998

Why is there a charge for this document?

Your purchase of this document contributes to the ongoing development of new and updated industry standards and publications. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards and publications development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low to allow as many companies as possible to participate. Therefore, the standards and publications revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards and publications, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit www.ipc.org or call 847/597-2872.

Thank you for your continued support.



#### IPC J-STD-001D

# Requirements for Soldered Electrical and Electronic Assemblies

A joint standard developed by the National Standard for Soldering Task Group (5-22a), and the Soldering Subcommittee (5-22) of the Assembly and Joining Processes Committee (5-20) of IPC



#### Supersedes:

J-STD-001C - March 2000 J-STD-001B - October 1996 J-STD-001A - April 1992

Incorporates modifications to noted errata.

Users of this publication are encouraged to participate in the development of future revisions.

#### Contact:

**IPC** 

3000 Lakeside Drive, Suite 309S Bannockburn, IL 60015-1219 Phone ( 847) 615-7100 Fax (847) 615-7105

#### ADOPTION NOTICE

J-STD-001, "Requirements for Soldered Electrical and Electronic Assemblies", was adopted on 19-JUL-01 for use by the Department of Defense (DoD). Proposed changes by DoD activities must be submitted to the DoD Adopting Activity: Commander, US Army Tank-Automotive and Armaments Command, ATTN: AMSTA-TR-E/IE, Warren, MI 48397-5000. Copies of this document may be purchased from the The Institute for Interconnecting and Packaging Electronic Circuits, 2215 Sanders Road, Northbrook, IL 60062-6135. http://www.ipc.org/

Custodians:

Army - AT Navy - AS

Reviewer Activities:

Adopting Activity:

Army - AT (Project SOLD-0059)

Army - AV, MI

AREA SOLD

<u>DISTRIBUTION STATEMENT A</u>: Approved for public release; distribution is unlimited.

## **Acknowledgment**

Members of the National Standard for Soldering Task Group (5-22a) have worked together to develop this document. We would like to thank them for their dedication to this effort. Any publication involving a complex technology draws material from a vast number of sources. While the principal members of the Joint National Standard for Soldering Task Group are shown below, it is not possible to include all of those who assisted in the evolution of this Standard. To each of them, the members of IPC extend their gratitude.

Assembly & Joining Processes Committee	National Standard for Soldering Task Group	Technical Liaisons of the IPC Board of Directors
Chair James F. Maguire Intel Corporation	Chair Teresa M. Rowe AAI Corporation	Peter Bigelow IMI Inc.
Vice Chair Leo P. Lambert	Vice Chair Daniel L. Foster	Sammy Yi Flextronics International

EPTAC Corporation	Soldering Technology International	Flextronics International	
National Standard for Soldering Task	k Group		
National Standard for Soldering Task Teresa M. Rowe, AAI Corporation Riley L. Northam, ACI/EMPF Leopold A. Whiteman, Jr., ACI/EMPF Constantino J. Gonzalez, ACME Training & Consulting Barry Morris, Advanced Rework Technology-A.R.T Debbie Wade, Advanced Rework Technology-A.R.T Joe Smetana, Alcatel Mark Shireman, Alliant Techsystems Inc. Terence Kern, Ambitech International Ronald McIlnay, American General Contracting	Gerald Leslie Bogert, Bechtel Plant Machinery, Inc. Thomas A. Woodrow, Ph.D., Boeing Phantom Works Thomas A. Carroll, Boeing Space Systems Kelly J. Miller, CAE Inc. Charles A. Lawson, CALCO Quality Services Sherman M. Banks, Calhoun Community College Gail Tennant, Celestica Lyle Q. Burhenn, Celestica Corporation Jason Bragg, Celestica International Inc.	Mary Muller, Eldec Corporation Werner Engelmaier, Engelmaier Associates, L.C. Leo P. Lambert, EPTAC Corporation Benny Nilsson, Ericsson AB Barrie D. Dunn, European Space Agency Gary M. Ferrari, C.I.D.+, Ferrari Technical Services Deepak K. Pai, C.I.D.+, General Dynamics-Advanced Information William Killion, Hella Electronics Corp. Kristen K. Troxel, Hewlett-Packard Company Ted S. Won, Honeywell Engines &	
Christopher Sattler, AQS - All Quality & Services, Inc.  Jennie S. Hwang, Asahi Technologies America, Inc.  William G. Butman, AssemTech Skills Training Corp.  Bill Strachan, AsTA - Highbury	<ul> <li>Adam R. Zbrzezny, Celestica International Inc.</li> <li>Juan Gamboa, Cisco Systems Inc.</li> <li>Graham Naisbitt, Concoat Limited</li> <li>Paul Lotosky, Cookson Electronics</li> <li>Jennifer Day, Current Circuits</li> <li>David B. Steele, Da-Tech Corp.</li> </ul>	Systems Heidi Jones, Honeywell Inc. William A. Novak, Honeywell Inc. John Pickett, Honeywell Inc. Joseph T. Slanina, Honeywell Inc. Dewey Whittaker, Honeywell Inc.	
College Ray Cirimele, B E S T Inc. James Jenkins, B E S T Inc. Robert Wettermann, B E S T Inc. Greg Hurst, BAE SYSTEMS Eugene R. Moyer, BAE Systems Steven W. Myers, BAE Systems William C. Dieffenbacher, BAE	Lowell Sherman, Defense Supply Center Columbus Glenn Dody, Dody Consulting William E. McManes, DRS Test & Energy Management Jon M. Roberts, DRS Test & Energy Management Peter Bratin, ECI Technology, Inc.	Don Youngblood, Honeywell Inc. Linda Tucker, Honeywell Technologies Solutions Inc. Fujiang Sun, Huawei Technologies Co., Ltd. James F. Maguire, Intel Corporation Mark A. Kwoka, Intersil Corporation Kenneth Reid, IUPUI-Indiana/Purdue University	

James Marsico, EDO Electronics

Richard W. Boerdner, EJE Research

Systems Group

Systems Platform Solutions

Joseph E. Kane, BAE Systems

Platform Solutions

Akikazu Shibata, Ph.D., Japan

Printed Circuit Association

- Blen F. Talbot, L-3 Communications Chanelle Smith, Lockheed Martin C. Dudley Hamilton, Lockheed
- Martin Aeronautics Co.
- Linda Woody, Lockheed Martin Electronics & Missiles
- Vijay Kumar, Lockheed Martin Missile & Fire Control
- Michael R. Green, Lockheed Martin Space Systems Company
- Hue T. Green, Lockheed Martin Space Systems Company
- Jeffery J. Luttkus, Lockheed Martin Space Systems Company
- David H. Ma, Lockheed Martin Space Systems Company
- Bruce D. Fischer, Logitech Inc.
- Russell H. Nowland, Lucent Technologies
- Helena Pasquito, M/A-COM Inc.
- Frank Durso, MacDermid, Inc.
- Gregg A. Owens, Manufacturing Technology Training Center
- James H. Moffitt, Moffitt Consulting Services
- Garry D. McGuire, Allied Aerospace
   NASA MSFC
- Robert D. Humphrey, NASA/ Goddard Space Flight Center
- Seppo J. Nuppola, Nokia Networks Oyj
- Ronald DePace, Northrop Grumman Mahendra S. Gandhi, Northrop Grumman
- Clarence W. Knapp, Northrop Grumman
- Randy McNutt, Northrop Grumman Phillip Chen, Northrop Grumman
- Canada Corporation Kevin Maelzer, Northrop Grumman
- Canada Corporation
  Alan S. Cash, Northrop Grumman
- Corporation
- Bernard Icore, Northrop Grumman Corporation
- Alvin R. Luther, Northrop Grumman Laser Systems

- Frederic W. Lee, Northrop Grumman Norden Systems
- William A. Rasmus, Jr., Northrop Grumman Space Systems
- Peggi J. Blakley, NSWC Crane
- Andrew W. Ganster, NSWC Crane
- William Dean May, NSWC Crane
- Rodney Dehne, OEM Worldwide
- Edward Zamborsky, OK International Inc.
- Ken A. Moore, Omni Training Corp.
- Peter E. Maher, PEM Consulting Rob Walls, C.I.D.+, PIEK
- International Education Centre BV
- Timothy M. Pitsch, Plexus Corp.
- Bonnie J. Gentile, Plexus NPI Plus -New England
- Guy M. Ramsey, R & D Assembly
- Mark Barnett, Raytheon Company
- Michael Blige, Raytheon Company Joe R. Felty, Raytheon Company
- David R. Nelson, Raytheon Company
- Fonda B. Wu, Raytheon Company
- Gordon Morris, Raytheon System Technology
- Steven A. Herrberg, Raytheon Systems Company
- Connie M. Korth, Reptron Manufacturing Services/Hibbing
- Susan S. Mansilla, Robisan Laboratory Inc.
- David C. Adams, Rockwell Collins
- David D. Hillman, Rockwell Collins
- Bryan James, Rockwell Collins
- Douglas O. Pauls, Rockwell Collins
- Donald H. Daebler, Ph.D., Sanmina-SCI
- Frank V. Grano, Sanmina-SCI Corporation
- Donna L. Lauranzano, Sanmina-SCI Corporation
- Kim MacDougall, Sanmina-SCI Corporation
- Kelly M. Schriver, Schriver Consultants

- Kevin J. Frasier, Scientific-Atlanta George Carroll, Siemens Energy & Automation
- Megan Shelton, Siemens Energy & Automation
- Bjorn Kullman, Sincotron Sverige AB
- Finn Skaanning, Skaanning Quality & Certification SQC
- Daniel L. Foster, Soldering Technology International
- Mel Parrish, Soldering Technology International
- Manon Dutil, Solectron Sherbrooke SSG
- Charles D. Fieselman, Solectron Technology Inc.
- Jasbir Bath, Solectron Technology Inc.
- Fortunata Freeman, Solectron Technology Inc.
- Sue Spath, Solectron Technology Inc.
- Xianyu Shea, Stryker Instruments
- John Mastorides, Sypris Electronics, LLC
- Raymond E. Dawson, Teamsource Technical Services
- Jay Messner, The Boeing Company
- Les Hymes, The Complete Connection
- Susan Roder, Thomas Electronics
- Debora L. Obitz, Trace Laboratories -East
- Martha Schuster, U.S. Army Aviation & Missile Command
- Sharon T. Ventress, U.S. Army Aviation & Missile Command
- Anthony M. Monteiro, United Technologies
- Constantin Hudon, Varitron Technologies Inc.
- Denis Barbini, Ph.D., Vitronics Soltec John S. Norton, Xerox Corporation

Steven T. Sauer, Xetron Corp.

## **Table of Contents**

1 G	ENERAL	1 3		MATERIALS, COMPONENTS AND EQUIPMENT REQUIREMENTS	_
1.1	Scope	1		Materials	
1.2	Purpose	1		Solder	
1.3	Classification	1	2 2.1		
1.4	Measurement Units and Applications	1	2.1 2.2		
1.4.1	Verification of Dimensions	1		Flux	
1.5	Definition of Requirements	1	3.1	Flux Application	
1.5.1	Hardware Defects and Process Indicators	2		Solder Paste	
1.5.2	Material and Process Nonconformance			Solder Preforms	
1.6	General Requirements			Adhesives	
1.7	Order of Precedence			Chemical Strippers	
1.7.1	Conflict			Heat Shrinkable Soldering Devices	
1.7.2	Clause References			Components	
1.7.3	Appendices	2	9.1	•	
1.8	Terms and Definitions	2	9.2	<b>,</b>	
1.8.1	Defect	2	9.3		
1.8.2	Disposition	2	9.4		
1.8.3	Electrical Clearance	2	9.5		
1.8.4	High Voltage	2	9.6		
1.8.5	Manufacturer (Assembler)	2	9.7		
1.8.6	Objective Evidence	2	10	Presoldering Cleanliness Requirements	
1.8.7	Process Control			Soldering Tools and Equipment	
1.8.8	Process Indicator	3			,
1.8.9	Proficiency	3		GENERAL SOLDERING AND ASSEMBLY REQUIREMENTS	7
1.8.10	Solder Destination Side	3 4.1	1	Electrostatic Discharge (ESD)	7
1.8.11	Solder Source Side	3 4.2	2	Facilities	
1.8.12	Supplier	3 4.2	2.1	Environmental Controls	7
1.8.13	User	3 4.2	2.2	Temperature and Humidity	7
1.9	Requirements Flowdown	3 4.2	2.3	Lighting	7
1.10	Personnel Proficiency	3 4.2	2.4	Field Assembly Operations	7
1.11	Acceptance Requirements	3 4.3	3	General Part Mounting Requirements	7
1.12	General Assembly Requirements	3 4.4	4	Hole Obstruction	8
1.13	Miscellaneous Requirements	3 4.5	5	Metal-Cased Component Isolation	8
1.13.1	Health and Safety	3 4.0	6	Adhesive Coverage Limits	8
1.13.2	Procedures for Specialized Technologies	3 4.7	7	Mounting of Parts on Parts (Stacking of	
2 A	PPLICABLE DOCUMENTS	4 40	0	Components)	
2.1	EIA	•••		Connectors and Contact Areas	
2.2	IPC			Handling of Parts	
2.3	Joint Industry Standards		9.1	Preheating	
2.3	ASTM		9.2	Č	
			9.3	, , , ,	
2.5	Electrostatic Discharge Association	5 4.9	9.4	Holding Devices and Materials	8

4.10	Heat Sinks	9	6.3	Supported Holes	17
4.11	Machine (Nonreflow) Soldering	9	6.3.1	Solder Application	17
4.11.1	Machine Controls	9	6.3.2	Through-Hole Component Lead Soldering	17
4.11.2	Solder Bath	9	7 SI	JRFACE MOUNTING OF COMPONENTS	18
4.12	Reflow Soldering	9	7.1	Surface Mount Device Lead Forming	
4.13	Intrusive Soldering (Paste-in-Hole)	9	7.1.1	Lead Deformation Limits	
4.14	Solder Connection	9	7.1.2	Flat Pack Parallelism	
4.14.1	Exposed Basis Metal	10	7.1.3	Surface Mount Device Lead Bends	
4.14.2	Exposed Surface Finishes	10	7.1.4	Flattened Leads	
4.14.3	Solder Connection Defects	10	7.1.5	Dual-in-Line Packages (DIPs)	
4.14.4	Partially Visible or Hidden Solder	10	7.1.6	Parts Not Configured for Surface Mounting	
	Connections	10	7.2	Devices with Externally Deposited Elements .	19
5 W	IRES AND TERMINAL CONNECTIONS	10	7.3	Leaded Component Body Clearing	
5.1	Wire and Cable Preparation	10	7.3.1	Axial-Leaded Components	
5.1.1	Tinning of Stranded Wire	10	7.4	Parts Configured for Butt Lead Mounting	
5.2	Solder Terminals	11	7.5	Hold Down of Surface Mount Leads	19
5.3	Bifurcated, Turret and Slotted Terminal	1.1	7.6	Soldering Requirements	20
<b></b> 0.4	Installation		7.6.1	Misaligned Components	20
5.3.1	Shank Damage		7.6.2	Unspecified and Special Requirements	
5.3.2	Flange Damage		7.6.3	Bottom Only Terminations	
5.3.3	Flared Flange Angles		7.6.4	Chip Components - Rectangular or	
5.3.4 5.3.5	Terminal Mounting - Mechanical  Terminal Mounting - Electrical			Square End Components - 1, 3 or 5 Side Termination	22
5.3.6	Terminal Soldering		7.6.5	Cylindrical End Cap (MELF) Terminations	
5.4	Mounting to Terminals		7.6.6	Castellated Terminations	
5.4.1	General Requirements		7.6.7	Flat, Ribbon, "L," and Gull Wing Leads	
5.4.2	Bifurcated and Turret Terminals		7.6.8	Round or Flattened (Coined) Leads	
5.4.3	Slotted Terminals		7.6.9	"J" Leads	
5.4.4	Hook Terminals		7.6.10	Butt Connections (Not Permitted for Class 3	21
5.4.5	Pierced or Perforated Terminals		7.0.10	Products)	28
5.4.6			7.6.11	Flat Lug Leads	29
	Cup and Hollow Cylindrical Terminals		7.6.12	Tall Profile Components Having Bottom	
5.5	Soldering to Terminals			Only Terminations	
5.5.1	Turret and Straight Pin Terminals		7.6.13	Inward Formed L-Shaped Ribbon Leads	31
5.5.2	Cup and Hollow Cylindrical Terminals	16	7.6.14	Surface Mount Area Array Packages	32
	ROUGH-HOLE MOUNTING AND		7.6.15	Quad Flat Pack (No Leads) (QFNL)	33
	ERMINATIONS		7.6.16	Components with Bottom Thermal Plane	24
6.1	Through-Hole Terminations - General			Terminations	34
6.1.1	Lead Forming		8 CI	LEANING PROCESS REQUIREMENTS	
6.1.2	Lead Deformation Limits		8.1	Cleanliness Exemptions	35
6.1.3	Lead Termination Requirements		8.2	Ultrasonic Cleaning	
6.1.4	Lead Trimming		8.3	Post-Solder Cleanliness	
6.1.5	Interfacial Connections	17	8.3.1	Particulate Matter	35
6.1.6	Coating Meniscus In Solder		8.3.2	Flux Residues and Other Ionic or Organic	25
6.2	Unsupported Holes	17	0.2.2	Contaminants	
6.2.1	Lead Termination Requirements for		8.3.3	Post-Soldering Cleanliness Designator	
	Unsupported Holes	17	8.3.4	Cleaning Option	35

8.3.5	Test for Cleanliness	35	APPENDIX		42
8.3.6	Testing	35		and Equipment	43
9 P	CB REQUIREMENTS	36	APPENDIX	C Material and Process Compatibility Testing	15
9.1	Printed Circuit Board Damage	36		_	7.7
9.1.1	Blistering/Delamination	36	APPENDIX	D Minimum Electrical Clearance - Electrical Conductor Spacing	47
9.1.2	Weave Exposure	36		-	.,
9.1.3	Haloing	36	APPENDIX	E Visual Comparisons of SnPb and Lead Free Solder Connections	49
9.1.4	Land Separation	36			.,
9.1.5	Land/Conductor Reduction in Size	37		Figures	
9.1.6	Flexible Circuitry Delamination	37		_	
9.1.7	Flexible Circuitry Damage	37	Figure 4-1	Hole Obstruction	
9.1.8	Burns	37	Figure 4-2	Acceptable Wetting Angles  Flange Damage	
9.1.9	Solder on Gold Contacts	37	Figure 5-1 Figure 5-2	Flare Angles	
9.1.10	Measles	37	Figure 5-2	Terminal Mounting - Mechanical	
9.2	Marking	37	Figure 5-4	Terminal Mounting - Nectrical	
9.3	Bow and Twist (Warpage)	37	Figure 5-5	Insulation Clearance Measurement	
10 (	COATING AND ENCAPSULATION	37	Figure 5-6	Service Loop for Lead Wiring	
10.1	Conformal Coating		Figure 5-7	Stress Relief Examples	13
10.1.1	Application		Figure 5-8	Continuous Runs	13
10.1.2	Performance Requirements		Figure 5-9	Wire and Lead Wrap Around	14
10.1.3	Conformal Coating Inspection		Figure 5-10	Side Route Connections and Wrap on	1 1
10.2	Encapsulation		Figure 5-11	Bifurcated Terminal  Top and Bottom Route Terminal Connection .	
10.2.1	Application		Figure 5-11	Hook Terminal Connections	
10.2.2	Performance Requirements		Figure 5-13	Pierced or Perforated Terminal Wire Wrap	
10.2.3	Rework of Encapsulant Material		Figure 6-1	Lead Bends	
10.2.4	Encapsulant Inspection		Figure 6-2	Vertical Fill Example	
	•		Figure 7-1	Surface Mount Device Lead Forming	18
	PRODUCT ASSURANCE		Figure 7-2	Surface Mount Device Lead Forming	18
11.1	Hardware Defects Requiring Disposition		Figure 7-3	Bottom Only Terminations	21
11.2	Inspection Methodology	39	Figure 7-4	Rectangular or Square End Components	22
11.2.1	Process Verification Inspection	39	Figure 7-5	MELF Terminations	23
11.2.2	Visual Inspection	39	Figure 7-6	Castellated Terminations	24
11.2.3	Sampling Inspection	39	Figure 7-7	Flat, Ribbon, "L," and Gull Wing Leads	25
11.3	Process Control Requirements	39	Figure 7-8	Round or Flattened (Coined) Leads	26
11.3.1	Opportunities Determination	40	Figure 7-9	"J" Leads	27
11.4	Statistical Process Control	40	Figure 7-10	Butt Joint	28
12 F	REWORK AND REPAIR	40	Figure 7-11	Flat Lug Leads	29
12.1	Rework of Unsatisfactory Solder	40	Figure 7-12	Tall Profile Components Having Bottom	~ ~
14.1	Connections	40	Eiguro 7 40	Only Terminations	
12.2	Repair		Figure 7-13	Inward Formed L-Shaped Ribbon Lead	
12.3	Post Rework/Repair Cleaning		Figure 7-14 Figure 7-15	BGA Solder Ball Spacing	
12.4	Rework of Conformal Coating/Encapsulant		Figure 7-15 Figure 7-16	PQFN  Component with Bottom Thermal Plane	33
			1 19ule /-10	Terminations	34
APPEN	NDIX A Summary of Criteria Requiring Disposition to Nonconforming		Figure E-1	SnPb Solder; No Clean Process	49
	Conditions	41	Figure E-2	SnAgCu Solder; No Clean Process	49

Figure E-3	SnPb Solder; Water Soluble Flux 49	Table 6-3	Protrusion of Leads in Supported Holes 17
Figure E-4	SnAgCu Solder; Water Soluble Flux 49	Table 6-4	Unsupported Holes with Component
Figure E-5	SnPb Solder; Water Soluble Flux 49		Leads, Minimum Acceptable Conditions 17
Figure E-6	SnAgCu Solder; Water Soluble Flux 49	Table 6-5	Supported Holes with Component Leads, Minimum Acceptable Conditions
Figure E-7	SnAgCu Solder; No Clean Process, N2 Reflow50	Table 7-1	SMT Lead Forming Minimum Lead Length 19
Figure E-8	SnAgCu Solder, No Clean Process;	Table 7-2	Surface Mount Components 20
iguic L o	Air Reflow50	Table 7-3	Dimensional Criteria - Bottom Only
Figure E-9	SnPb Solder; No Clean Process 50		Terminations
Figure E-10	SnAgCu Solder; No Clean Process 50	Table 7-4	Dimensional Criteria - Chip Components - Rectangular or Square End Components -
igure E-11	SnPb Solder; No Clean Process 50		1, 3 or 5 Side Termination
Figure E-12	SnAgCu Solder; No Clean Process 50	Table 7-5	Dimensional Criteria - Cylindrical End Cap
Figure E-13	SnPb Solder 51		(MELF) Terminations
Figure E-14	SnAgCu Solder 51	Table 7-6	Dimensional Criteria - Castellated
Figure E-15	SnPb Solder51	T-1-1-77	Terminations
Figure E-16	SnAgCu Solder 51	Table 7-7	Dimensional Criteria - Flat, Ribbon, "L," and Gull Wing Leads
Figure E-17	SnPb Solder; OSP Finish 51	Table 7-8	Dimensional Criteria - Round or Flattened
Figure E-18	SnAgCu Solder; OSP Finish 51		(Coined) Leads
Figure E-19	SnAgCu Solder 52	Table 7-9	Dimensional Criteria - "J" Leads
Figure E-20	SnAgCu Solder 52	Table 7-10	Dimensional Criteria - Butt/I Connections
Figure E-21	SnAgCu Solder 52		(Not Applicable to Class 3)
Figure E-22	SnAgCu Solder 52	Table 7-11	Dimensional Criteria - Flat Lug Leads
		Table 7-12	Dimensional Criteria - Tall Profile Components Having Bottom Only
	Tables		Terminations
Table 1-1	Design and Fabrication Specification	Table 7-13	Dimensional Criteria - Inward Formed L-Shaped Ribbon Leads
Table 3-1	Solder Limits for Tin/Lead Alloys 5	Table 7-14	Dimensional Criteria - Area Array/Ball
Table 4-1	Solder Acceptability, Intrusive Soldering,		Grid Array
	Supported Holes	Table 7-15	Dimensional Criteria - PQFN
Table 5-1	Damaged Strand Limits 11	Table 7-16	Dimensional Criteria - Bottom Thermal
Table 5-2	Terminal Soldering Requirements 12	T.11. 0.4	Plane Terminations
Table 5-3	Staking Requirements of Side Route	Table 8-1	Designation of Surfaces to be Cleaned
	Straight Through Connections - Bifurcated Terminals	Table 8-2	Cleanliness Testing Designators
Table 5-4	Solder Height Requirements Wire to Post 15	Table 10-1	Coating Thickness
Table 6-1	Lead Bend Radius	Table 11-1	Magnification Aid Applications for Solder Connections
Table 6-2	Protrusion of Leads in Unsupported Holes 17	Table 11-2	Magnification Aid Applications - Other 39

# Requirements for Soldered Electrical and Electronic Assemblies

#### 1 GENERAL

**1.1 Scope** This standard prescribes practices and requirements for the manufacture of soldered electrical and electronic assemblies. Historically, electronic assembly (soldering) standards contained a more comprehensive tutorial addressing principles and techniques. For a more complete understanding of this document's recommendations and requirements, one may use this document in conjunction with IPC-HDBK-001, IPC-A-610 and IPC-HDBK-610.

When J-STD-001 is cited or required by contract, the requirements of IPC-A-610 do not apply unless separately or specifically required. When IPC-A-610 is cited along with J-STD-001, the order of precedence is to be defined in the procurement documents.

- **1.2 Purpose** This standard describes materials, methods and acceptance criteria for producing soldered electrical and electronic assemblies. The intent of this document is to rely on process control methodology to ensure consistent quality levels during the manufacture of products. It is not the intent of this standard to exclude any procedure for component placement or for applying flux and solder used to make the electrical connection.
- **1.3 Classification** This standard recognizes that electrical and electronic assemblies are subject to classifications by intended end-item use. Three general end-product classes have been established to reflect differences in producibility, complexity, functional performance requirements, and verification (inspection/test) frequency. It should be recognized that there may be overlaps of equipment between classes.

The user (see 1.8.13) is responsible for defining the product class. The product class should be stated in the procurement documentation package.

#### **CLASS 1 General Electronic Products**

Includes products suitable for applications where the major requirement is function of the completed assembly.

#### **CLASS 2 Dedicated Service Electronic Products**

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically the end-use environment would not cause failures.

#### **CLASS 3 High Performance Electronic Products**

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

- 1.4 Measurement Units and Applications All dimensions and tolerances, as well as other forms of measurement (temperature, weight, etc.) in this standard are expressed in SI (System International) units (with Imperial English equivalent dimensions provided in brackets). Dimensions and tolerances use millimeters as the main form of dimensional expression; micrometers are used when the precision required makes millimeters too cumbersome. Celsius is used to express temperature. Weight is expressed in grams.
- **1.4.1 Verification of Dimensions** Actual measurement of specific part mounting and solder fillet dimensions and determination of percentages are not required except for referee purposes. For the purposes of determining conformance to this specification, all specified limits in this standard are absolute limits as defined in ASTM E29.
- **1.5 Definition of Requirements** The word **shall** is used in the text of this document wherever there is a requirement for materials, preparation, process control or acceptance of a soldered connection.

Where the word **shall** leads to a hardware defect for at least one class, the requirements for each class are annotated in text boxes located adjacent to that occurrence in the text. These boxes are summarized in Appendix A. Appendix A identifies each listed condition for each class as either "Defect," "Process Indicator," "Acceptable," or "No Requirement Established." In case of a discrepancy between requirements in the text boxes and Appendix A, requirements listed in the text boxes take precedence.

Line drawings and illustrations are depicted herein to assist in the interpretation of the written requirements of this standard. Text takes precedence over the figures.

IPC-HDBK-001, a companion document to this specification, contains valuable explanatory and tutorial information compiled by IPC Technical Committees that is relative to this specification. Although the Handbook is not a part of this specification, when there is confusion over the specification verbiage, the reader is referred to the Handbook for assistance.

**1.5.1** Hardware Defects and Process Indicators Hardware characteristics or conditions that do not conform to the requirements of this specification are classified as either hardware defects or hardware process indicators. Hardware

defects listed in the applicable text boxes **shall**<sup>1</sup> be identified, documented, and dispositioned, e.g., rework, scrap, use as is, repair.

(1) Class 1-Defect Class 2-Defect Class 3-Defect

Not all process indicators specified by this standard are listed in the text boxes. Hardware process indicator data should be monitored (see 11.3), but the hardware need not be dispositioned.

It is the responsibility of the user (see 1.8.13) to define additional or unique defect categories applicable to the product. It is the responsibility of the manufacturer (see 1.8.5) to identify defects and process indicators that are unique to the assembly process (see 1.13.2).

**1.5.2 Material and Process Nonconformance** Hardware found to be produced using either materials or processes that do not conform to the requirements of this standard **shall**<sup>2</sup> be dispositioned when the condition is a defect listed in the applicable text box. This disposition **shall**<sup>2</sup> address the potential effect of the nonconfor-

the potential effect of the nonconformance on functional capability of the hardware such as reliability and design life (longevity).

(2) Class 1-Defect Class 2-Defect Class 3-Defect

**Note:** Material and process nonconformance differs from hardware defects or hardware process indicators in that the material/process nonconformance often does not result in an obvious change in the hardware's appearance but can impact the hardware's performance; e.g., contaminated solder, incorrect solder alloy (per drawing/procedure).

**1.6 General Requirements** Use of this standard requires agreement on the class to which the product belongs. If the user and manufacturer do not establish and document the acceptance class, the manufacturer may do so.

Surface mount designs need to undergo 'Design for Reliability' procedures based on the design parameters, the use conditions, the design life, and the acceptable failure risk to assure the designs capability to reliably function for its intended use. For "Design for Reliability" information see IPC-D-279 and IPC-9701.

The soldering operations, equipment, and conditions described in this document are based on electrical/ electronic circuits designed and fabricated in accordance with the specifications listed in Table 1-1.

**1.7 Order of Precedence** The contract always takes precedence over this standard, referenced standards and drawings.

Table 1-1 Design and Fabrication Specification

Board Type	Design Specification	Fabrication Specification
Generic Requirements	IPC-2221	IPC-6011
Rigid Printed Boards	IPC-2222	IPC-6012 <sup>1</sup> IPC-A-600
Flexible Circuits	IPC-2223	IPC-6013
Rigid Flex Board	IPC-2223	IPC-6013

**Note 1.** This document takes exception to the bare board measling criteria of IPC-A-600G, Clause 2.3.1, and IPC-6012, Clause 3.3.2.1.

**1.7.1 Conflict** In the event of conflict between the requirements of this standard and the applicable assembly drawing(s)/documentation, the applicable user approved assembly drawing(s)/documentation govern. In the event of a conflict between the text of this standard and the applicable documents cited herein, the text of this standard takes precedence. In the event of conflict between the requirements of this standard and an assembly drawing(s)/documentation that has not been user approved, this standard governs.

When IPC J-STD-001 is cited or required by contract, the requirements of IPC-A-610 do not apply unless separately or specifically required. When IPC-A-610 or other related documents are cited along with IPC J-STD-001, the order of precedence is to be defined in the procurement documents.

- **1.7.2 Clause References** When a clause in this document is referenced, its subordinate clauses also apply.
- **1.7.3 Appendices** Appendices to this Standard are not requirements unless separately and specifically required by the applicable contracts, assembly drawing(s), documentation or purchase order.
- **1.8 Terms and Definitions** Other than those terms listed below, the definitions of terms used in this standard are in accordance with IPC-T-50.
- **1.8.1 Defect** A nonconformance to the requirements of this standard (listed in or referenced by Appendix A) or other risk factors as identified by the manufacturer (see 1.8.5).
- **1.8.2 Disposition** The determination of how defects should be treated. Dispositions include, but are not limited to, rework, use as is, scrap or repair.
- **1.8.3 Electrical Clearance** The minimum spacing between noncommon uninsulated conductors (e.g., patterns, materials, hardware, residue) is referred to as "minimum electrical clearance" throughout this document and is defined in the applicable design standard or on the approved or controlled documentation. Insulating material

needs to provide sufficient electrical isolation. In the absence of a known design standard use Appendix D (derived from IPC-2221). Any violation of minimum electrical clearance as a result of nonconformance to defined criteria is a defect condition.

- 1.8.4 High Voltage The term "high voltage" will vary by design and application. The high voltage criteria in this document are only applicable when specifically required in the drawings/procurement documentation.
- 1.8.5 Manufacturer (Assembler) The individual, organization, or company responsible for the assembly process and verification operations necessary to ensure full compliance of assemblies to this standard.
- **1.8.6 Objective Evidence** Documentation in the form of hard copy, computer data, video, or other media.
- 1.8.7 Process Control A system or method to continually steer an operation in reducing variation in the processes or products to meet or exceed the goal in quality and performance.
- **1.8.8 Process Indicator** A detectable anomaly, other than a defect, that is attributable to variation in material, equipment operation, workmanship or processes.
- 1.8.9 Proficiency The capability to perform tasks in accordance with the requirements and verification procedures detailed in this standard.
- 1.8.10 Solder Destination Side The solder destination side is that side of the printed circuit board (PCB) that the solder flows toward in a through-hole application.
- 1.8.11 Solder Source Side The solder source side is the side of the PCB to which solder is applied.
- 1.8.12 Supplier The individual, organization or company which provides the manufacturer (assembler) components (electronic, electromechanical, mechanical, printed boards, etc.) and/or materials (solder, flux, cleaning agents, etc.).
- 1.8.13 User The individual, organization, company, contractually designated authority, or agency responsible for the procurement of electrical/electronic hardware, and having the authority to define the class of equipment and any variation or restrictions to the requirements of this standard (i.e., the originator/custodian of the contract detailing these requirements).
- 1.9 Requirements Flowdown When this standard is contractually required, the applicable requirements of this standard (including product class - see 1.3) shall<sup>1</sup> be imposed on all applicable subcon-

(1) Class 1-Defect Class 2-Defect Class 3-Defect tracts, assembly drawing(s), documentation and purchase orders. Unless otherwise specified the requirements of this standard are not imposed on the procurement of commercial-off-the-shelf (COTS or catalog) assemblies or subassemblies.

When a part is adequately defined by a specification, then the requirements of this standard should be imposed on the manufacture of that part only when necessary to meet enditem requirements. When it is unclear where flowdown should stop, it is the responsibility of the manufacturer to establish that determination with the user.

1.10 Personnel Proficiency All instructors, operators, and inspection personnel shall<sup>2</sup> be proficient in the tasks to be performed. Objective evidence of that proficiency shall<sup>2</sup> be maintained and be available for review. Objective evidence should include records of training to the applicable job functions being performed, work experience, testing to

the requirements of this standard, and/or results of periodic reviews of proficiency. Supervised on-the-job training is acceptable until proficiency is demonstrated.

(2) Class 1-Not Est Class 2-Defect Class 3-Defect

#### 1.11 Acceptance Requirements

All products shall<sup>3</sup> meet the requirements of the assembly drawing(s)/ documentation and the requirements for the applicable product class specified herein.

(3) Class 1-Defect Class 2-Defect Class 3-Defect (4) Class 1-Not Est Class 2-Defect Class 3-Defect

Manufacturers shall<sup>4</sup> perform 100% inspection unless sampling inspection is defined as part of a documented process control plan (see 11.2.2).

1.12 General Assembly Requirements The electrical and mechanical integrity of components and assemblies

shall<sup>5</sup> be retained after exposure to processes employed during manufacture and assembly (e.g., handling, baking, fluxing, soldering, and cleaning).

(5) Class 1-Defect Class 2-Defect Class 3-Defect

#### 1.13 Miscellaneous Requirements

- 1.13.1 Health and Safety The use of some materials referenced in this standard may be hazardous. To provide for personnel safety, follow the applicable local and Federal Occupational, Safety and Health Regulations.
- 1.13.2 Procedures for Specialized Technologies As an industry consensus standard, this document cannot address all of the possible components and product design combinations, e.g., magnetic windings, high frequency, high voltage, etc. Where uncommon or specialized technologies are used, it may be necessary to develop unique process and/or acceptance criteria. Often, unique definition is necessary to

consider the specialized characteristics while considering product performance criteria.

The development should include user involvement. The acceptance criteria shall have user agreement. Mounting and soldering requirements for specialized processes and/or technologies not specified herein shall<sup>2</sup> be performed in accordance with documented procedures which are available for review.

(1) Class 1-Not Est Class 2-Not Est Class 3-Defect (2) Class 1-Not Est Class 2-Defect Class 3-Defect

Whenever possible these criteria should be submitted to the IPC Technical Committee to be considered for inclusion in upcoming revisions of this standard.

### 1.13.2.1 Manufacture of Devices Incorporating Mag-

netic Windings This standard is very limited in its applicability to the manufacturing processes associated with the mounting of internal electronic elements and the soldering of the internal connections of transformers, motors, and similar devices. Unless a user has a specific need for the controls provided by this standard, it should not be imposed relative to the manufacture of the internal ele-

ments of these devices. The external interconnect points (e.g., terminals, pins, etc.) shall<sup>3</sup> meet the solderability requirements of this document, less steam aging.

(3) Class 1-Defect Class 2-Defect Class 3-Defect

1.13.2.2 High Frequency Applications High frequency applications (i.e., radio wave and microwaves) may require part clearances, mounting systems, and assembly designs which vary from the requirements stated herein.

1.13.2.3 High Voltage Applications High voltage applications may require part clearances, mounting systems, and assembly designs which vary from the (4) Class 1-Defect

requirements stated herein. Class 2-Defect Class 3-Defect

There shall<sup>4</sup> be no broken strands for wires used at a potential of 6kV or greater.

#### 2 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the invitation for bid, form a part of this specification extent specified herein.

#### 2.1 EIA1

EIA-557-1 Statistical Process Control Guidance for Selection of Critical Manufacturing Operations for Use Implementing an SPC System for Passive Components

IPC-HDBK-001 Requirements for Soldered Electrical Electronic Assemblies Handbook

**IPC-A-36** Cleaning Alternatives Board

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

**IPC-A-600** Acceptability of Printed Boards

**IPC-A-610** Acceptability of Electronic Assemblies

**IPC-OI-645** Standard for Visual Optical Inspection Aids

**IPC-SM-785** Guidelines for Accelerated Reliability Testing of Surface Mount Attachments

IPC-TM-650 Test Methods Manual<sup>3</sup>

- 2.3.25 Detection and Measurement of Ionizable Surface Contaminants
- 2.3.27 Cleanliness Test Residual Rosin
- 2.3.28 Ionic Analysis of Circuit Boards Ion Chromatography Method
- 2.3.38 Surface Organic Contamination Detection
- 2.3.39 Surface Organic Contamination Identification Test (Infrared Analytical Method)
- 2.4.22 Bow and Twist
- 2.6.3 Moisture and Insulation Resistance, Rigid, Rigid/Flex and Flex Printed Wiring Boards
- 2.6.3.3 Moisture and Surface Insulation Resistance, Fluxes

IPC-SM-817 General Requirements for Dielectric Surface Mounting Adhesives

IPC-CC-830 Qualification and Performance of Electrical Insulating Compound for Printed Board Assemblies

IPC-2221 Generic Standard on PWB Design

IPC-2222 Sectional Standard on Rigid PWB Design

IPC-2223 Sectional Design Standard for Flexible Printed **Boards** 

IPC-6011 Generic Performance Specification of Printed Boards

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

IPC-6013 Qualification and Performance for Flexible Printed Boards

<sup>2.2</sup> IPC<sup>2</sup>

<sup>1.</sup> www.eia.org

<sup>2.</sup> www.ipc.org

<sup>3.</sup> Current and revised IPC Test Methods are available through IPC-TM-650 subscription and on the IPC website (www.ipc.org/html/testmethods.htm).

**IPC-7095** Design and Assembly Process Implementation for BGAs

**IPC-9191** General Guidelines for Implementation of Statistical Process Control (SPC)

**IPC-9201** Surface Insulation Resistance Handbook

**IPC-9261** In-Process DPMO and Estimated Yield for PWAs

#### 2.3 Joint Industry Standards<sup>4</sup>

**IPC/EIA J-STD-002** Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

**J-STD-003** Solderability Tests for Printed Boards

**J-STD-004** Requirements for Soldering Fluxes

**J-STD-005** Requirements for Soldering Paste

**J-STD-006** Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

**IPC/JEDEC J-STD-020** Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices

**IPC/JEDEC J-STD-033** Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

**IPC/JEDEC-9701** Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

#### 2.4 ASTM<sup>5</sup>

**ASTM E29** Standard Practice for Using Significant Digits in Test Data to Determine Conformance with Specifications

#### 2.5 Electrostatic Discharge Association<sup>6</sup>

**ANSI/ESD-S-20.20** Protection of Electrical and Electronic Parts, Assemblies and Equipment

# 3 MATERIALS, COMPONENTS AND EQUIPMENT REQUIREMENTS

**3.1 Materials** The materials and processes used to assemble/manufacture electronic assemblies **shall**<sup>1</sup> be selected such that (1) Class 1-Defect

assemblies **shall**<sup>1</sup> be selected such that their use, in combination, produce products acceptable to this standard.

(1) Class 1-Defect Class 2-Defect Class 3-Defect When major elements of the proven processes are changed, (e.g., flux, solder paste, cleaning media or system, solder alloy or soldering system) validation of the acceptability of the change(s) **shall**<sup>2</sup> be performed and documented. They

can also pertain to a change in bare board supplier, solder resist or metallization. An example of a method for accomplishing this is provided as Appendix C.

(2) Class 1-Not Est Class 2-Not Est Class 3-Defect

**3.2 Solder** Solder alloys **shall**<sup>3</sup> be in accordance with J-STD-006 or equivalent. Solder alloys other than Sn60A, Pb36B, and Sn63A which provide the required electrical and mechanical attributes may be used if all other conditions of this standard are met and objective evidence of

such is available for review. Flux that is part of flux-cored solder wire **shall**<sup>3</sup> meet the requirements of 3.3. Flux percentage is optional.

(3) Class 1-Defect Class 2-Defect Class 3-Defect

**3.2.1 Solder - Lead Free** Solder alloys less than 0.1% lead by weight not listed by J-STD-006 may be used when such use is agreed upon by the manufacturer and the user.

#### 3.2.2 Solder Purity Maintenance Solder used for pre-

conditioning, gold removal, tinning of parts, and machine soldering **shall**<sup>4</sup> be analyzed, replaced or replenished at a frequency to ensure compliance with the limits specified in Table 3-1.

(4) Class 1-Not Est Class 2-Defect Class 3-Defect

Table 3-1 Solder Limits<sup>1</sup> for Tin/Lead Alloys

	Maximum Contaminant Limit (%) <sup>2</sup>			
Contaminant	Preconditioning (Lead/Wire Tinning)	Assembly Soldering (Pot, Wave, etc.)		
Copper	0.750	0.300		
Gold	0.500	0.200		
Cadmium	0.010	0.005		
Zinc	0.008	0.005		
Aluminum	0.008	0.006		
Antimony	0.500	0.500		
Iron	0.020	0.020		
Arsenic	0.030	0.030		
Bismuth	0.250	0.250		
Silver <sup>3</sup>	0.750	0.100		
Nickel	0.025	0.010		

Note 1. The tin content of the solder bath shall<sup>4</sup> be within ± 1.5% of nominal for the solder specified and tested at the same frequency as testing for copper/ gold contamination. The balance of the bath shall<sup>4</sup> be lead or the items listed above.

Note 2. The total copper, gold, cadmium, zinc and aluminum contaminants shall not<sup>4</sup> exceed 0.4% for assembly soldering.

Note 3. Not applicable for Pb36B: limits to be 1.75% to 2.25%.

<sup>4.</sup> www.ipc.org

<sup>5.</sup> www.astm.org

<sup>6.</sup> www.esda.org

Solder alloys other than Sn60A, Sn63A, or Pb36B tin/lead solders shall be in compliance with equivalent documented limits.

If contamination exceeds the limits, intervals between the analyses, replacement or replenishment shall be shortened. The frequency of analysis should be determined on the basis of historical data, or monthly analyses. Records containing the results of all analyses and solder bath usage

(e.g., total time in use, amount of replacement solder, or area throughput) shall<sup>1</sup> be maintained for a minimum of one year for each process/ system.

(1) Class 1-Not Est Class 2-Defect Class 3-Defect

3.3 Flux Flux shall<sup>2</sup> be in accordance with J-STD-004 or equivalent.

Flux shall<sup>3</sup> conform to flux activity levels L0 and L1 of flux materials rosin (RO), resin (RE), or organic (OR), except organic flux activity (2) Class 1-Defect Class 2-Defect Class 3-Defect

(3) Class 1-Not Est Class 2-Not Est Class 3-Defect

level L1 shall not<sup>3</sup> be used for no-clean soldering.

When other activity levels or flux materials are used, data demonstrating compatibility shall<sup>3</sup> be available for review (see 3.1).

Flux or solder paste soldering process combinations previously tested or qualified in accordance with other specifications do not require additional testing.

Type H or M fluxes shall not<sup>2</sup> be used for tinning of stranded wires.

3.3.1 Flux Application When an external flux is used in conjunction with flux cored solders, the fluxes shall<sup>4</sup> be compatible.

(4) Class 1-Defect Class 2-Defect Class 3-Defect

**3.4 Solder Paste** Solder paste **shall**<sup>5</sup> be in accordance with J-STD-005 or equivalent. Solder paste shall<sup>5</sup> also meet the requirements of 3.2 and 3.3.

(5) Class 1-Defect Class 2-Defect Class 3-Defect

3.5 Solder Preforms Solder preforms **shall**<sup>6</sup> meet the requirements of 3.2 and 3.3.

(6) Class 1-Defect Class 2-Defect Class 3-Defect

3.6 Adhesives Electrically nonconductive adhesive materials used for attachment of components should conform to an acceptable document or standard, e.g., IPC-SM-

817, or as otherwise specified. The adhesives selected shall not<sup>7</sup> be detrimental to the component or assembly they are used on. The material shall<sup>7</sup> be cured.

(7) Class 1-Defect Class 2-Defect Class 3-Defect 3.7 Chemical Strippers Chemical solutions, pastes, and

creams shall not<sup>8</sup> cause damage or degradation. Chemical strippers shall **not**<sup>8</sup> be used with stranded wires.

(8) Class 1-Defect Class 2-Defect Class 3-Defect

3.8 Heat Shrinkable Soldering **Devices** Heat shrinkable soldering devices shall<sup>9</sup> be installed in accordance with the requirements of the

(9) Class 1-Defect Class 2-Defect Class 3-Defect

device manufacturer unless otherwise specified. See 8.1 for cleaning requirements.

3.9 Components Components (e.g., electronic devices, mechanical parts, printed boards) selected for assembly shall<sup>10</sup> be compatible with all materials and processes, e.g., temperature ratings, used to manufacture the assembly/product.

(10) Class 1-Defect Class 2-Defect Class 3-Defect

Moisture sensitive components (as classified by IPC/ JEDEC J-STD-020 or other documented classification procedure) shall 10 be handled in a manner consistent with IPC/JEDEC J-STD-033 or other documented procedure.

3.9.1 Solderability Electronic/mechanical components (including PCBs) and wires to be soldered shall<sup>11</sup> meet the solderability requirements of J-STD-002 or equivalent and printed boards shall<sup>11</sup> meet the requirements of J-STD-003 or equivalent. When a solderability inspection operation or

pretinning and inspection operation is performed as part of the documented assembly process, that operation may be used in lieu of solderability testing (see 3.9.2).

(11) Class 1-Defect Class 2-Defect Class 3-Defect

3.9.2 Solderability Maintenance

The manufacturer **shall**<sup>12</sup> ensure that all components, parts, leads, wiring, terminals, and printed boards that (12) Class 1-Defect Class 2-Defect Class 3-Defect

have met the requirements of 3.9.1 are solderable at the start of hand and/or machine soldering operations. The manufacturer should establish procedures to minimize part solderability degradation (see IPC-HDBK-001).

- **3.9.3 Gold Removal** Gold **shall** <sup>13</sup> be removed:
- From at least 95% of the surface to be soldered of the through-hole component leads with 2.5 µm [0.0984 mil] or more of gold.

(13) Class 1-Not Est Class 2-Proc Ind Class 3-Defect

- From 95% of all surfaces of surface mount components to be soldered regardless of gold thickness.
- From the surface of solder terminals plated with 2.5 µm [0.0984 mil] or more of gold.

A double tinning process or dynamic solder wave may be used for gold removal.

Electroless nickel immersion gold (ENIG) finishes on PCBs are exempt from this requirement.

These requirements may be eliminated if there is documented objective evidence available for review that there are no gold related solder embrittlement problems associated with the soldering process being used.

3.9.4 Rework of Nonsolderable Parts A component lead, termination, or board not conforming to the solderability requirements of 3.9.1 may be reworked (e.g., by dipping in hot solder) before soldering.

During tinning of leads, heat sinks shall be attached to the leads of components that are heat sensitive. A reworked part shall1 conform to the

(1) Class 1-Defect Class 2-Defect Class 3-Defect

requirements of 3.9.1, less steam conditioning.

3.9.5 Component and Seal Damage Part bodies and lead seals shall **not**<sup>2</sup> be degraded below the part specification requirements.

(2) Class 1-Defect Class 2-Defect Class 3-Defect

3.9.6 Component Damage Minor surface flaws, discoloration, meniscus cracks, or chips are acceptable. However, they shall not<sup>3</sup> expose the component substrate or active element nor affect structural integrity. There shall not<sup>3</sup> be any damage to components in excess

of component specification limits. Components shall not<sup>3</sup> be charred. Visible cracks on glass-to-metal seals are not acceptable.

(3) Class 1-Defect Class 2-Defect Class 3-Defect

**Note:** Visual aids can be found in IPC-A-610.

3.9.7 Coating Meniscus Component coating meniscus shall not<sup>4</sup> be trimmed.

(4) Class 1-Not Est Class 2-Defect Class 3-Defect

- 3.10 Presoldering Cleanliness Requirements The assembly should be clean of any matter that will inhibit compliance to the requirements of this standard.
- 3.11 Soldering Tools and Equipment Tools and equipment used shall<sup>5</sup> be selected and maintained such that no damage or degradation that would be detrimental to the designed function of parts or assemblies result from their use. Soldering irons, equipment, and systems shall<sup>5</sup> be chosen and employed to provide temperature control and isolation from electrical overstress or ESD (see 4.1). A tool

used to cut leads shall not<sup>5</sup> impart shock that damages a component lead seal or internal connection. See Appendix B for guidelines on tool selection and maintenance.

(5) Class 1-Defect Class 2-Defect Class 3-Defect 4 GENERAL SOLDERING AND ASSEMBLY REQUIRE-**MENTS** 

4.1 Electrostatic Discharge (ESD) If any ESD susceptible devices are employed, the manufacturer shall<sup>6</sup> establish and implement a documented ESD control program in accordance with ANSI/ESD-20.20 or

as otherwise specified. Documentation necessary for an effective program **shall**<sup>6</sup> be available for review.

(6) Class 1-Defect Class 2-Defect Class 3-Defect

**4.2 Facilities** Cleanliness and ambient environments in all work areas shall<sup>7</sup> be maintained at levels that prevent

contamination or deterioration of soldering tools, materials, and surfaces to be soldered. Eating, drinking, and/or use of tobacco products shall<sup>7</sup> be prohibited in the work area.

(7) Class 1-Defect Class 2-Defect Class 3-Defect

- 4.2.1 Environmental Controls The soldering facility should be enclosed, temperature and humidity controlled, and maintained at a positive pressure.
- 4.2.2 Temperature and Humidity When humidity decreases to a level of 30% or lower, the manufacturer shall<sup>8</sup> verify that electrostatic discharge control is adequate, and that the range of humidity in the assembly area is sufficient to allow soldering and assembly materials to function correctly in the process, based on vendor recommendations or documented evidence of process performance. For operator comfort and solderability maintenance, the temperature should be maintained between 18°C

[64.4°F] and 30°C [86°F] and the relative humidity should not exceed 70%. For process control, more restrictive temperature and humidity limits may be required.

trolled environment on the operation

being performed on the hardware.

(8) Class 1-Not Est Class 2-Defect Class 3-Defect

- 4.2.3 Lighting Illumination at the surface of workstations should be 1000 lm/m<sup>2</sup> minimum. Light sources should be selected to prevent shadows.
- 4.2.4 Field Assembly Operations In field assembly operations on Class 3 products where the controlled environmental conditions required by this standard cannot be effectively achieved, precautions shall<sup>9</sup> be taken to maximize the quality of solder connections (9) Class 1-Not Est and minimize the effects of the uncon-

Class 2-Not Est Class 3-Defect

4.3 General Part Mounting Requirements When design restrictions mandate mounting components incapable of withstanding soldering temperatures incident to a particular

process, such components shall<sup>1</sup> be mounted and soldered to the assembly as a separate operation.

(1) Class 1-Defect Class 2-Defect Class 3-Defect

If cleaning is required, parts **shall**<sup>1</sup> be mounted with sufficient clearances between the body and the PCB to assure adequate cleaning and cleanliness testing. Assemblies should be cleaned after each soldering operation so that subsequent placement and soldering operations are not impaired by contamination (see 8, Cleanliness Process Requirements).

On assemblies using mixed component mounting technology, through-hole components should be mounted on one side of the printed board. Surface mounted components may be mounted on either or both sides of the assembly.

Parts should be mounted such that part markings and reference designators are visible (see 9.2).

**4.4 Hole Obstruction** Parts and components shall<sup>2</sup> be

mounted such that they do not obstruct solder flow onto the solder destination side lands of platedthrough holes (PTHs) required to be soldered (see Figure 4-1 and 4.14.3).

(2) Class 1-Accept Class 2-Proc Ind Class 3-Defect

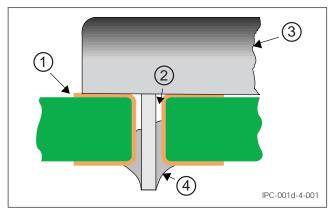


Figure 4-1 Hole Obstruction

- 1. Hard mount 2. Air
- 3. Component body
- Solder

4.5 Metal-Cased Component Isolation Metal-cased

components shall<sup>3</sup> be isolated from adjacent electrically conductive elements.

(3) Class 1-Defect Class 2-Defect Class 3-Defect

4.6 Adhesive Coverage Limits Adhesive materials,

when used, shall not4 preclude the formation of an acceptable solder connection. Adhesive materials extending from under SMT components shall **not**<sup>5</sup> be visible in the termination area. Adhesives, e.g., staking, bonding. shall not<sup>4</sup> contact an unsleeved area of a sleeved glass body component.

(4) Class 1-Defect Class 2-Defect Class 3-Defect (5) Class 1-Accept Class 2-Proc Ind Class 3-Defect

4.7 Mounting of Parts on Parts (Stacking of Components) When part stacking is permitted by the assembly

drawing(s)/documentation, parts shall **not**<sup>6</sup> violate minimum electrical clearance between other parts or components.

(6) Class 1-Defect Class 2-Defect Class 3-Defect

4.8 Connectors and Contact Areas

face(s) of connectors or contact areas intended for electrical connection shall<sup>7</sup> be free of contaminants or foreign material.

(7) Class 1-Defect Class 2-Defect Class 3-Defect

The mating sur-

4.9 Handling of Parts Parts shall<sup>8</sup> be handled in a manner to preclude damage to terminations and to avoid the need for subsequent lead straightening operations. Once parts are mounted on printed boards, the unsoldered assembly shall<sup>8</sup> be handled, transported (e.g., hand or conveyor) and processed in a manner to preclude movement that would detrimentally affect formation of acceptable solder connections. When parts are mounted in solder paste, the unsoldered assembly should be processed so that the part does not move within the solder paste such that the final soldered connection results in part misalignment exceeding

the requirements of Section 7. After soldering operations have been performed, the assembly shall<sup>8</sup> be sufficiently cooled so the solder is solidified prior to further handling.

(8) Class 1-Defect Class 2-Defect Class 3-Defect

**4.9.1 Preheating** For other than hand soldering, assemblies should be preheated to minimize the presence of volatile solvents prior to exposure to molten solder to reduce thermal shock to boards and components, to improve sol-

der flow, and to reduce the solder dwell time. The preheat temperature exposure shall not9 degrade printed boards, components, or soldering performance.

(9) Class 1-Defect Class 2-Defect Class 3-Defect

**4.9.2 Controlled Cooling** Controlled cooling may be used. If used, controlled (accelerated (10) Class 1-Not Est

or slowed ramp) cooling shall<sup>10</sup> be in accordance with documented procedures.

Class 2-Defect Class 3-Defect

- **4.9.3 Drying/Degassing** Prior to soldering, the assembly may be treated to reduce detrimental moisture and other volatiles.
- 4.9.4 Holding Devices and Materials Equipment, devices, materials, or techniques used to handle boards or retain parts and components to the printed boards through

any and all stages of soldering shall not<sup>1</sup> contaminate, damage, or degrade printed boards or components. The equipment, devices, materials or techniques should be adequate to maintain

(1) Class 1-Defect Class 2-Defect Class 3-Defect

4.10 Heat Sinks When hand soldering a component identified as heat sensitive, a thermal shunt or heat sink shall<sup>2</sup> be attached to the device lead between the area to be soldered and the component body to minimize com-

component positioning and permit sol-

der flow through plated-through holes

and/or onto terminal areas.

ponent heating.

identified.

(2) Class 1-Defect Class 2-Defect Class 3-Defect

#### 4.11 Machine (Nonreflow) Soldering

**4.11.1 Machine Controls** The manufacturer shall<sup>3</sup> maintain operating procedures describing the soldering process and the proper operation of the automatic soldering machine and associated equipment.

For the soldering machine, these procedures, as a minimum, shall<sup>3</sup> define the preheat temperature, flux application procedures and coverage, solder temperature, controlled atmosphere (if used), rate of travel, frequency of temperature verification measurements, and frequency of solder bath analysis.

If any of the above mentioned characteristics require an adjustment for a different printed circuit assembly, drawing number, or other positive identification element, the setting to be utilized shall<sup>3</sup> be

(3) Class 1-Not Est Class 2-Defect Class 3-Defect

4.11.2 Solder Bath The period of exposure of any printed board to a solder bath shall<sup>4</sup> be limited to a duration that will not degrade the board or parts mounted thereon. The solder bath temperature, based on the solder alloy in use, shall<sup>5</sup> be set at a predetermined value with a tolerance of  $\pm$  5°C [ $\pm$  9°F].

(4) Class 1-Defect Class 2-Defect Class 3-Defect (5) Class 1-Not Est Class 2-Defect Class 3-Defect

4.11.2.1 Solder Bath Maintenance Solder bath purity in machine soldering of printed board assemblies shall<sup>6</sup> be maintained in accordance with 3.2.2. Dross shall<sup>6</sup> be

removed from the solder bath in a manner that assures that dross does not contact the items being soldered. Automatic or manual methods for dross removal are acceptable.

(6) Class 1-Not Est Class 2-Not Est Class 3-Defect

4.12 Reflow Soldering The manufacturer **shall**<sup>7</sup> develop and maintain operating procedures describing the reflow soldering process and the

(7) Class 1-Not Est Class 2-Defect Class 3-Defect

proper operation of the equipment. These procedures shall<sup>7</sup> include, as a minimum, a reproducible time/temperature envelope including the flux and solder paste application procedures and coverage, drying/degassing operation (when required), preheating operation (when required), controlled atmosphere (if used), solder reflow operation, and a cooling operation (see 4.9.2). These steps may be part of an integral or in-line system or may be accomplished through a series of separate operations.

4.13 Intrusive Soldering (Paste-in-Hole) These criteria apply to reflow soldering of through-hole connections.

Solder shall<sup>8</sup> be applied to the assembly such that the reflowed solder connections of the through hole connections, meet the requirements of Table 4-1.

(8) Class 1-Defect Class 2-Defect Class 3-Defect

4.14 Solder Connection All solder connections shall<sup>9</sup> indicate evidence of wetting and adherence where the solder blends to the soldered surface. The solder connections should have a generally smooth

appearance. Marks or scratches in the solder connection shall not<sup>9</sup> degrade the integrity of the connection.

(9) Class 1-Defect Class 2-Defect Class 3-Defect

There are solder alloy compositions, component lead and terminal finishes, or printed board platings and special soldering processes (e.g., slow cooling with large mass PCBs)

Table 4-1 Solder Acceptability, Intrusive Soldering, Supported Holes<sup>1</sup>

Criteria	Class 1	Class 2	Class 3
A. Vertical fill of solder. <sup>2</sup>	Not Specified	75%	75%
B. Wetting on solder source side of lead and barrel. <sup>3</sup>	270°	270°	330°
C. Percentage of land area covered with wetted solder on solder source side. <sup>3</sup>	75%	75%	75%
D. Fillet and wetting on solder destination side of lead and barrel.	Not Specified	180°	270°
Percentage of land area covered with wetted solder on solder destination side.	0	0	0

Note 1. Wetted solder refers to solder applied by the solder process.

Note 2. The 25% unfilled height includes both source and destination side depressions.

Note 3. Applies to any side to which solder paste was applied.

that may produce dull, matte, satin, gray, or grainy appearing solders that are normal for the material or process involved. These solder connections are acceptable.

Wetting cannot always be judged by surface appearance. The wide range of solder alloys in use may exhibit from low or near zero degree contact angles to nearly 90° contact angles as typical. The acceptable solder connection **shall**<sup>1</sup> indicate evidence of wetting and adherence where the solder blends to the soldered surface. The solder connection wetting angle (solder to component and solder to PCB termination) **shall not**<sup>1</sup> exceed 90° (Figure 4-2 A, B). As an exception, the solder connection to a termination

may exhibit a wetting angle exceeding 90° (Figure 4-2 C, D) when it is created by the solder contour extending over the edge of the solderable termination area or solder resist.

(1) Class 1-Defect Class 2-Defect Class 3-Defect

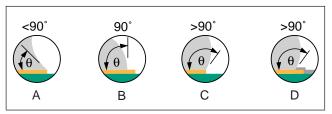


Figure 4-2 Acceptable Wetting Angles

The primary difference between the solder connections created with processes using tin-lead alloys and processes using lead free alloys is related to the visual appearance of the solder. All other solder fillet criteria are the same. The photographs in Appendix E illustrate acceptable solder connections with various solder alloys and process conditions.

Lead-free and tin-lead connections may exhibit similar appearances but lead free alloys are more likely to have surface roughness (grainy or dull) or different wetting contact angles.

- **4.14.1 Exposed Basis Metal** Exposed basis metal on leads or lands is acceptable provided it is not part of the required fillet area. These surfaces typically include, but are not limited to, component lead ends and the edges and/or periphery of printed board lands and conductors.
- **4.14.2 Exposed Surface Finishes** Exposed surface finish on leads or lands is acceptable provided it is not part of the required fillet area.
- **4.14.3 Solder Connection Defects** The following solder connection conditions **shall**<sup>2</sup> be considered defects:

  (2) Class 1-Defect Class 2-Defect

Class 3-Defect

- a. Fractured solder connections.
- b. Disturbed solder connections.
- c. Cold solder connections.
- d. Solder that violates minimum electrical clearance (e.g.,

- bridges), or contacts the component body (except as noted in 7.6.7 and 7.6.8).
- e. Fails to comply with wetting criteria of 4.14.
- Solder bridging between connections except when path is present by design.

#### 4.14.4 Partially Visible or Hidden Solder Connections

Partially visible or hidden solder connections are acceptable provided that the following conditions are met:

- a. The design does not restrict solder flow to any connection element on the solder destination side lands (e.g., PTH component) of the assembly.
- b. The visible portion, if any, of the connection on either side of the PTH solder connection (or the visible portion of the SMD connection) is acceptable.
- Process controls are maintained in a manner assuring repeatability of assembly techniques.

#### **5 WIRES AND TERMINAL CONNECTIONS**

**5.1 Wire and Cable Preparation** Insulation discoloration resulting from thermal stripping is permissible, however,

the insulation **shall not**<sup>3</sup> be charred. Chemical insulation stripping agents **shall**<sup>3</sup> be used only for solid wire and are to be neutralized or removed prior to soldering.

(3) Class 1-Defect Class 2-Defect Class 3-Defect

(4) Class 1-Accept Class 2-Defect Class 3-Defect

The number of damaged (nicked or broken) strands in a single wire **shall not**<sup>3</sup> exceed the limits given in Table 5-1. There **shall**<sup>4</sup> be no birdcaging allowed beyond the outside diameter of the insulation. (Recommendations and requirements on wires used in high voltage applications are provided in 1.13.2.3.)

- **5.1.1 Tinning of Stranded Wire** Portions of stranded wire that will be soldered **shall**<sup>5</sup> be tinned prior to mounting when:
- Wires will be formed for attachment to solder terminals.
- Wires will be formed into splices (other than mesh).

Solder wicking **shall not**<sup>6</sup> extend to a portion of the wire which is required to remain flexible. The solder **shall**<sup>5</sup> wet the tinned portion of the wire and should penetrate to the inner strands of the wire.

(5) Class 1-Not Est Class 2-Defect Class 3-Defect

(6) Class 1-Defect Class 2-Defect Class 3-Defect

Stranded wires **shall not**<sup>5</sup> be tinned when:

- Wires will be used in crimp terminations.
- Wires will be used in threaded fasteners.
- Wires will be used in forming mesh splices.
- Wires will be used in heat shrinkable solder device.

Table 5-1 Damaged Strand Limits

		=	
Number of Strands	Maximum Allowable Strands, Scraped, Nicked or Severed for Class 1,2	Maximum Allowable Strands, Scraped, Nicked or Severed for Class 3 for Wires that will not be Tinned Before Installation	Maximum Allowable Strands, Scraped, Nicked or Severed for Class 3 for Wires that will be Tinned Prior to Installation
Less than 7	0	0	0
7-15	1	0	1
16-25	3	0	2
26-40	4	3	3
41-60	5	4	4
61-120	6	5	5
121 or more	6%	5%	5%

Note 1: No damaged strands for wires used at a potential for 6 kV or greater.

Note 2: For plated wires, a visual anomaly that does not expose basis metal is not considered to be strand damage.

5.2 Solder Terminals Terminals and solder cups shall not1 be modified to accept oversize conductors.

(1) Class 1-Not Est Class 2-Defect Class 3-Defect

#### 5.3 Bifurcated, Turret and Slotted Terminal Installation

5.3.1 Shank Damage The shank shall not<sup>2</sup> have circumferential cracks or splits, regardless of extent. The shank of the terminal shall not<sup>2</sup> be perforated, split, cracked, or oth-

erwise damaged to the extent that oils, flux, inks, or other liquid substances utilized for processing the printed board can be entrapped within the mounting hole.

(2) Class 1-Defect Class 2-Defect Class 3-Defect

**5.3.2 Flange Damage** The rolled or flared area of the flange shall<sup>3</sup> be free of missing pieces, circumferential splits or cracks.

The rolled or flared area of the flange shall<sup>3</sup> have no more than three radial splits or cracks provided that the splits or cracks are separated by at least 90° and do not extend into the barrel of the terminal (see Figure 5-1).

The flange shall not<sup>3</sup> be split, cracked or otherwise damaged to the extent that flux, oils, inks, or other liquid substances utilized for processing the printed board can be entrapped within the mounting hole.

(3) Class 1-Defect Class 2-Defect Class 3-Defect

5.3.3 Flared Flange Angles Flared flanges should be formed to an included angle of between 35° and 120° and should extend between 0.4 mm [0.0157 in] and 1.5 mm [0.0591 in] beyond the surface of the land. Minimum electrical clearance shall<sup>4</sup> be maintained and the flare diameter should not exceed the diameter of the land (see Figure 5-2).

(4) Class 1-Defect Class 2-Defect Class 3-Defect

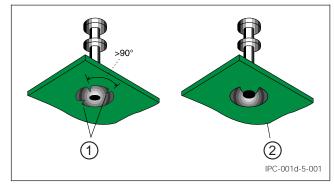


Figure 5-1 Flange Damage

- 1. Radial split (3 max)
- 2. Split extends into barrel

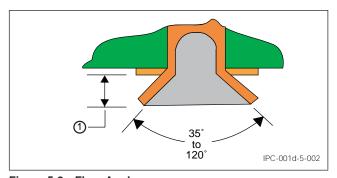


Figure 5-2 Flare Angles

1. 0.4 mm [0.0157 in] min to 1.5 mm [0.0591 in] max

5.3.4 Terminal Mounting - Mechanical Terminals not connected to printed circuit or ground planes shall<sup>5</sup> be of the rolled flange configuration (see Figure 5-3). A printed

foil land may be used as a seating surface for a rolled flange provided that the land is isolated and not connected to an active printed circuit or ground plane.

(5) Class 1-Not Est Class 2-Defect Class 3-Defect

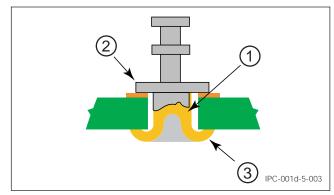


Figure 5-3 Terminal Mounting - Mechanical

- 1. Shank
- 2. Flat shoulder
- 3. Rolled flange

**5.3.5 Terminal Mounting - Electrical** Terminals **shall**<sup>1</sup> be mounted with flared flanges in noninterfacial PTHs pro-

vided the mounting is in conjunction with a land or ground plane on the flared side as shown in Figure 5-4A. Terminals **shall not**<sup>1</sup> be flared to the base material of the printed board.

(1) Class 1-Not Est Class 2-Defect Class 3-Defect

Terminals may be mounted in non-PTHs with active circuitry on the top side and a roll flange on the back side of the board (see Figure 5-4B).

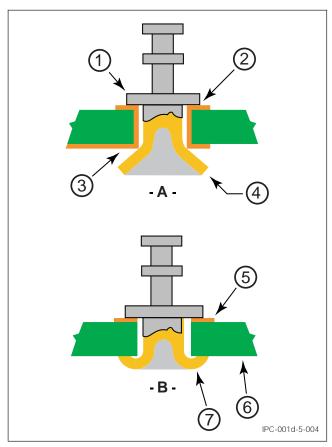


Figure 5-4 Terminal Mounting - Electrical

- 1. Flat shoulder
- 2. Nonfunctional land
- 3. Plated-through hole
- 4. Flared flange
- 5. Conductor
- 6. Board
- 7. Rolled flange

**5.3.6 Terminal Soldering** Terminals mounted in accordance with 5.3, and soldered to the printed board in unsupported holes or noninterfacial PTHs should exhibit evi-

dence of good wetting to both the terminal flange/shoulder and land or conductive plane. The soldered connection **shall**<sup>2</sup> meet the requirements shown in Table 5-2.

(2) Class 1-Defect Class 2-Defect Class 3-Defect

Table 5-2 Terminal Soldering Requirements

Criteria	Class 1	Class 2	Class 3
A. Circumferential fillet and wetting - solder source side	270°	270°	330°
B. Percentage of solder source side land area covered with wetted solder	75%	75%	75%

#### 5.4 Mounting to Terminals

**5.4.1 General Requirements** Unless otherwise defined, the requirements for mounting apply to both wires and component leads (see 5.1).

**5.4.1.1 Insulation Clearance (C)** The clearance (C) (Figure 5-5) between the end of the insulation and the solder of the connection **shall not**<sup>3</sup> permit shorting or violation of minimum electrical clearance between noncommon conductors. The clearance between the end of wire insulation and the solder of the connection is as follows:

a. Minimum Clearance: The insulation is in contact with

the solder connection but **shall not**<sup>4</sup> interfere with formation of the fillet. The contour of the wires should not be obscured at the termination of the insulation.

b. Maximum Clearance: Clearance shall<sup>5</sup> be two wire diameters (including insulation) or 1.5 mm [0.0591 in], whichever is larger.

- (3) Class 1-Defect Class 2-Defect Class 3-Defect
- (4) Class 1-Accept Class 2-Defect Class 3-Defect
- (5) Class 1-Accept Class 2-Proc Ind Class 3-Defect

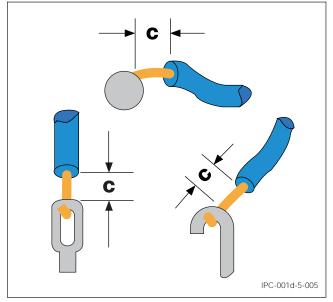


Figure 5-5 Insulation Clearance Measurement

**5.4.1.2 Service Loops** Lead wires **shall**<sup>1</sup> be dressed in

the proper position with a slight loop or gradual bend as shown in Figure 5-6. The bend should be sufficient to allow at least one field repair.

(1) Class 1-Not Est Class 2-Proc Ind Class 3-Defect

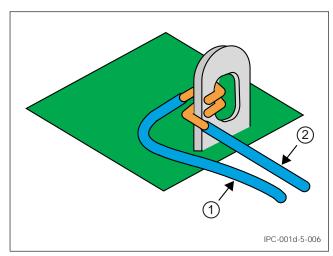


Figure 5-6 Service Loop for Lead Wiring

- 1. Acceptable
- 2. Not acceptable (insufficient)

5.4.1.3 Stress Relief Component leads shall<sup>2</sup> have stress relief. Wires connected to terminals shall<sup>3</sup> have stress relief (see Figure 5-7).

- (2) Class 1-Defect Class 2-Defect Class 3-Defect
- (3) Class 1-Accept Class 2-Proc Ind Class 3-Defect

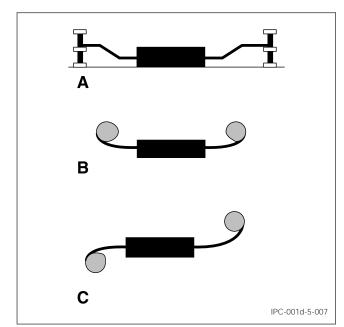


Figure 5-7 Stress Relief Examples

5.4.1.4 Orientation of Lead or Wire Wrap Attachments to terminals that require a wrap may be wrapped clockwise or counterclockwise (consistent with the direction of potential stress application). The lead or wire shall<sup>4</sup> continue the curvature of the dress of the lead/wire and shall not<sup>4</sup> interfere with the wrapping of other leads or wires on the terminal or overlap itself or each other.

(4) Class 1-Accept Class 2-Proc Ind Class 3-Defect

5.4.1.5 Continuous Runs A continuous solid bus wire may be run from terminal to terminal if three or more

bifurcated, turret, or pierced terminals are to be connected (see Figure 5-8). A curvature shall<sup>5</sup> be included in the unwrapped wire portion of the jumper to provide relief of tension from environmental loading. The following additional requirements shall<sup>6</sup> be met:

- (5) Class 1-Defect Class 2-Defect Class 3-Defect
- (6) Class 1-Accept Class 2-Proc Ind Class 3-Defect
- a. The connection to the first and last terminals meet the required wrap for individual terminals.
- b. For each intermediate turret terminal, the wire is wrapped around or interweaves each terminal.
- c. For each intermediate bifurcated terminal, the wire passes through the slot and is in contact with the base of the terminal or a previously installed wire.
- d. For each intermediate pierced or perforated terminal, the wire is in contact with at least two nonadjacent contact surfaces of each intermediate terminal.

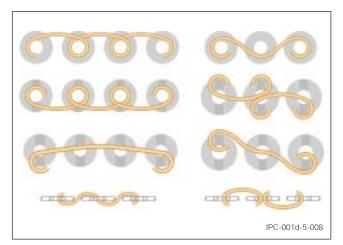


Figure 5-8 **Continuous Runs** 

5.4.1.6 Insulation Sleeving (Wires Soldered to Pierced, Hook and Cup Terminals) When insulation sleeving is installed over a wire soldered to a pierced, hook or cup terminal, there shall<sup>7</sup> be no damage to the sleeving that would allow shorting of the wire or violation of minimum electrical clearance to adjacent circuitry.

The sleeving shall<sup>8</sup> fit snugly and extend over the insulation a minimum of 6.0 mm [0.236 in], or two wire diameters, whichever is greater, and extend over the terminal beyond the solder termination.

- (7) Class 1-Defect Class 2-Defect Class 3-Defect
- (8) Class 1-Accept Class 2-Defect Class 3-Defect

5.4.1.7 Lead and Wire End Extensions The lead and

wire ends should not extend beyond the terminal more than one (1) lead diameter. Minimum electrical clearance requirements **shall**<sup>1</sup> be met.

(1) Class 1-Defect Class 2-Defect Class 3-Defect

#### 5.4.2 Bifurcated and Turret Terminals

**5.4.2.1** Wire and Lead Wrap-Around - Turret and Straight Pin Leads and wires should be mechanically secured to their terminals before soldering. Such mechanical securing should prevent movement between the parts of

the connection during the soldering operation. Leads and wires **shall**<sup>2</sup> have a minimum of 180° contact between the wire/lead and the terminal. Leads and wires **shall not**<sup>3</sup> have less than 90° of contact between the wire and the terminal. (see Figure 5-9).

(2) Class 1-Accept Class 2-Proc Ind Class 3-Defect

(3) Class 1-Defect Class 2-Defect Class 3-Defect

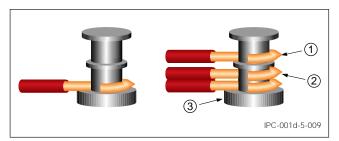


Figure 5-9 Wire and Lead Wrap Around

- 1. Upper guide slot
- 2. Lower guide slot
- 3. Base

**5.4.2.2 Termination of Small Gauge Wire (AWG 30 and Smaller)** As an exception to the requirements of 5.4.2.1,

wire size AWG 30 or smaller **shall**<sup>4</sup> be wrapped at least once and should be wrapped no more than three complete turns around the terminal.

(4) Class 1-Accept Class 2-Proc Ind Class 3-Defect

#### 5.4.2.3 Side Route Connection - Bifurcated Terminals

When practical, except for bus wire, wires should be placed in ascending order with the largest on the bottom. Lead and wire ends may extend beyond the base of terminals provided the minimum electrical clearance is maintained. The attachments should be maintained such that clearance between wires and clearance between the wires and the terminal board or panel is a minimum consistent with the wire insulation thickness.

For side route connections wrapped to a post on the terminal, the wire or component lead **shall**<sup>5</sup> be dressed through the slot. Wires may be wrapped to

(5) Class 1-Defect

either post of the terminal, assuring positive contact of the wire with at least one corner of the post (see Fig(5) Class 1-Defect Class 2-Defect Class 3-Defect ure 5-10). There **shall**<sup>6</sup> be positive contact of the wire with at least one corner of the post (Figure 5-10) and a minimum 90° contact between the wires/leads and the terminal. As an exception Class 1 and Class 2 assemblies, wires/leads 0.75 mm [0.0295 in] or larger may be routed straight through.

Table 5-3 provides the staking criteria for side route connections that do not meet minimum wrap criteria. Wires or

leads **shall**<sup>6</sup> extend beyond the post of the terminal and be in contact with the base of the terminal or the previously installed wire.

(6) Class 1-Accept Class 2-Proc Ind Class 3-Defect

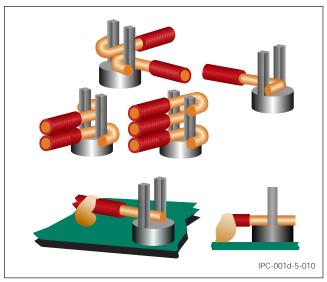


Figure 5-10 Side Route Connections and Wrap on Bifurcated Terminal

Table 5-3 Staking Requirements of Side Route Straight Through Connections - Bifurcated Terminals

Wire Diameter	Class 1	Class 2	Class 3
All wire sizes			Defect if not staked
<0.75 mm [0.0295 in] <sup>1</sup>	Defect if r		
≥0.75 mm [0.0295 in] <sup>1</sup>	Acceptable if not staked	Process Indicator if not staked	

Note 1: Equivalent to AWG 22.

**5.4.2.4 Top and Bottom Route Connections** Bottom routed wires **shall**<sup>7</sup> be wrapped on the terminal base or post with a minimum of 90° bend (see Figure 5-11). Wire insulation **shall not**<sup>7</sup> enter the base of post of terminal. When top routed wires to bifurcated terminals are required by the design, the wire **shall**<sup>7</sup> feed straight into the terminal

between the tines. Remaining space between the tines **shall**<sup>7</sup> be filled by having the wire bent double or by using a separate filler wire (see Figure 5-11).

(7) Class 1-Accept Class 2-Proc Ind Class 3-Defect

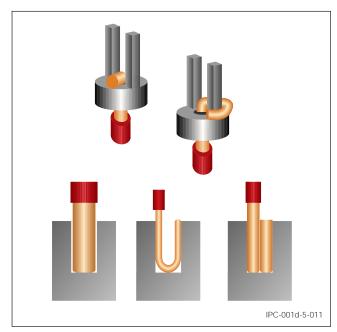


Figure 5-11 Top and Bottom Route Terminal Connection

**5.4.3 Slotted Terminals** Slotted terminals **shall**<sup>1</sup> be terminated with the lead/wire extending straight through the

opening of the terminal with no wrap. The lead/wire end **shall**<sup>1</sup> be discernable on the exit side of the terminal and **shall**<sup>2</sup> not violate minimum electrical clearance. Solder as a minimum **shall**<sup>2</sup> wet 100% of the portion of the lead/wire that is in contact with the

(1) Class 1-Accept Class 2-Proc Ind Class 3-Defect

(2) Class 1-Defect Class 2-Defect Class 3-Defect

terminal. Solder may completely fill the slot.

#### 5.4.4 Hook Terminals

- a. Wire(s) shall<sup>3</sup> be wrapped 180° minimum.
- b. Wire(s) **shall**<sup>3</sup> be no closer than one wire diameter to the end of the hook.
- c. Wire(s) should be within the arc of the hook (see Figure 5-12).
- d. For components using hook terminations, wires **shall**<sup>4</sup> be spaced a minimum of two lead diameters or 1.0 mm [0.039 in], whichever is greater, from the base of the terminal.
- (3) Class 1-Accept Class 2-Defect Class 3-Defect
  - (4) Class 1-Accept Class 2-Proc Ind Class 3-Defect

**5.4.5 Pierced or Perforated Terminals** For wiring to a single terminal, the wire(s) **shall**<sup>5</sup> pass through the eye and contact two nonadjacent sides of the terminal or be wrapped around the terminal a minimum of 90° (see Figure 5-13).

For user approved designs that incorporate staking/bonding of wires, the wire(s) attached to pierced terminals **shall**<sup>5</sup> contact at least two surfaces of the terminal.

(5) Class 1-Accept Class 2-Defect Class 3-Defect

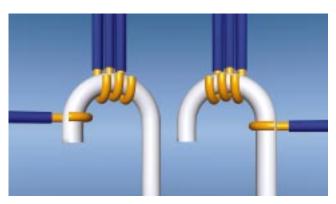


Figure 5-12 Hook Terminal Connections

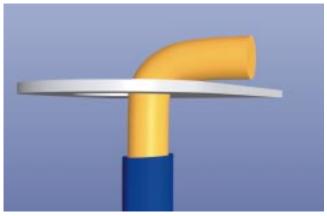


Figure 5-13 Pierced or Perforated Terminal Wire Wrap

5.4.6 Cup and Hollow Cylindrical Terminals The strands of any wire shall<sup>6</sup> meet the requirements of 5.1. The wire or wires shall<sup>7</sup> be inserted for the full depth of the cup.

(6) Class 1-Accept Class 2-Proc Ind Class 3-Defect

(7) Class 1-Not Est Class 2-Proc Ind Class 3-Defect

**5.5 Soldering to Terminals** A solder fillet **shall<sup>8</sup>** join the wire/lead to the terminal. Leads with a wrap of 180° or greater **shall<sup>8</sup>** show evidence of good wetting for a minimum of 75% of the minimum required wrap area. Straight

through terminations or leads wrapped less than 180° **shall**<sup>8</sup> show evidence of good wetting for 100% of the lead to terminal contact area.

(8) Class 1-Defect Class 2-Defect Class 3-Defect

**5.5.1 Turret and Straight Pin Terminals** Wetted solder in the wire to post contact area **shall**<sup>9</sup> conform to Table 5-4.

Table 5-4 Solder Height Requirements Wire to Post

	Class 1	Class 2	Class 3
Depression of solder between the post and the lead/wire is not greater than	50	9%	25%

#### 5.5.2 Cup and Hollow Cylindrical Terminals

- a. A fillet **shall**<sup>1</sup> be formed along the surfaces of contact between the wire and terminal.
- b. Solder shall<sup>2</sup> fill at least 75% of terminals.
- c. Any solder buildup on the outside of the cup shall not<sup>2</sup> affect form, fit or function.
- d. Solder **shall**<sup>1</sup> wet the entire inside of a terminal.
- e. Solder **shall**<sup>1</sup> be visible in the inspection hole and may rise slightly above it. Solder may overfill the cup.
- (1) Class 1-Not Est Class 2-Proc Ind Class 3-Defect (2) Class 1-Defect

Class 2-Defect

Class 3-Defect

#### **6 THROUGH-HOLE MOUNTING AND TERMINATIONS**

**6.1 Through-Hole Terminations - General** Axial Leaded components, when mounted horizontal to the board surface, should be approximately centered between the mounting holes. The entire length of the component body should be in contact with the board surface. The maximum space between the component body and the board **shall**<sup>3</sup> not exceed 0.7 mm [0.028 in]. Components that are required to be mounted off the board **shall**<sup>4</sup> be elevated at least 1.5 mm [0.059 in]. Components mounted in unsupported holes and required to be elevated **shall**<sup>4</sup> be provided with lead forms at the board surface, or other mechanical support.

Axial leaded components mounted vertically in unsupported holes **shall**<sup>4</sup> be mounted with lead forms or other

mechanical support. Axial lead components mounted vertically in supported holes **shall**<sup>4</sup> have component height requirements (from the board to the body or weld bead) in accordance with the user determined dimension.

(3) Class 1-Not Est Class 2-Not Est Class 3-Proc Ind

(4) Class 1-Defect Class 2-Defect Class 3-Defect

**6.1.1 Lead Forming** Part and component leads should be preformed to the final configuration excluding the final clinch or retention bend before assembly or installation. The lead forming process **shall not**<sup>5</sup> damage lead seals, welds, or connections internal to components.

Leads **shall**<sup>6</sup> extend at least one lead diameter or thickness but not less than 0.8 mm [0.031 in] from the body or weld before the start of the bend radius (see Figure 6-1).

The lead bend radius **shall**<sup>6</sup> be in accordance with Table 6-1.

**Note:** Measurement is made from the end of the part. (The end of the part is defined to include any coating, solder seal, solder or weld bead, or any other extension.)

(5) Class 1-Defect Class 2-Defect Class 3-Defect

(6) Class 1-Accept Class 2-Proc Ind Class 3-Defect

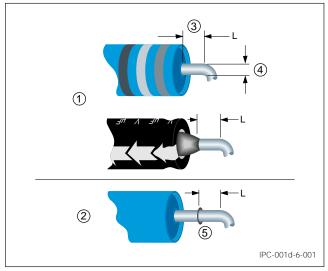


Figure 6-1 Lead Bends

- 1. Standard bend
- 2. Welded bend
- Straight for 1 diameter/lead thickness, but not less than 0.8 mm [0.031 in]
- 4. Diameter/Thickness
- 5. Weld

Table 6-1 Lead Bend Radius

Lead Diameter	Minimum Bend Radius (R)
Less than to 0.8 mm [0.031 in]	1 diameter/thickness
From 0.8 to 1.2 mm [0.031 to 0.047 in]	1.5 diameters/thickness
Greater than 1.2 mm [0.047 in]	2 diameters/thickness

**6.1.2 Lead Deformation Limits** Leads **shall not**<sup>7</sup> have nicks or deformation exceeding 10% of the diameter,

width, or thickness of the lead except as allowed for flattened leads (see 7.1.4). Exposed basis metal is acceptable provided it does not prevent the

(7) Class 1-Defect Class 2-Defect Class 3-Defect

formation of an acceptable solder connection.

**6.1.3 Lead Termination Requirements** Component leads in supported holes may be terminated using a straight through, partially clinched, or clinched configuration. The clinch should be sufficient to provide mechanical restraint during the soldering process. The orientation of the clinch relative to any conductor is optional. DIP leads should have at least two diagonally opposing leads partially bent outward.

Class 3 lead terminations in unsupported holes **shall**<sup>8</sup> be clinched a minimum of 45°.

If a lead or wire is clinched, the lead **shall**<sup>8</sup> be wetted in the clinched area. The outline of the lead should be discernible in the solder connection.

(8) Class 1-Not Est Class 2-Not Est Class 3-Defect

Tempered leads shall not<sup>1</sup> be terminated with a (full) clinched configuration.

Lead protrusion shall not<sup>1</sup> violate minimum electrical clearance requirements. Lead protrusion shall<sup>1</sup> be in accordance with Table 6-2 for unsup-

(1) Class 1-Defect Class 2-Defect Class 3-Defect

ported holes or Table 6-3 for supported holes.

Table 6-2 Protrusion of Leads in Unsupported Holes

	Class 1	Class 2	Class 3
(L) min.	End is discernible in solder <sup>1</sup>		Sufficient to clinch
(L) max.1	No danger of shorts <sup>2</sup>		

Note 1. Lead protrusion should not exceed 2.5 mm [0.0984 in] if there is a possibility of violation of minimum electrical spacing, damage to soldered connections due to lead deflection or penetration of static protective packaging during subsequent handling or operating environments.

Note 2. See 6.2.1.

Table 6-3 Protrusion of **Leads in Supported Holes** 

	Class 1	Class 2	Class 3	
(L) min.	End is discernible in solder <sup>1</sup>			
(L) max. <sup>2</sup>	No danger of shorts	2.5 mm [0.0984 in]	1.5 mm [0.0591 in]	

Note 1. For boards greater than 2.3 mm [0.0986 in] thick, with components having preestablished lead lengths, e.g., DIPs, sockets, connectors, as a minimum component or lead shoulder need to be flush to the board surface, but lead end may not be visible in the subsequent solder connection

Note 2. Lead protrusion should not exceed 2.5 mm [0.0984 in] if there is a possibility of violation of minimum electrical spacing, damage to soldered connections due to lead deflection or penetration of static protective packaging during subsequent handling or operating environments

Connector leads are exempt from the maximum length requirement provided that they do not violate minimum electrical spacing at the next higher assembly level.

6.1.4 Lead Trimming Leads may be trimmed after soldering provided the cutters do not damage the component or solder connection due to physical shock. Tempered leads shall not<sup>2</sup> be trimmed unless specified on the drawings.

When lead cutting is performed after soldering, the solder terminations shall<sup>3</sup> either be reflowed or visually inspected at 10X to ensure that the original solder connection has not been damaged (e.g., fractured) or deformed. If the solder

connection is reflowed this is considered part of the soldering process and not rework. This requirement does not apply to components which are designed such that a portion of the lead is intended to be removed after soldering (e.g., break-away tie bars).

(2) Class 1-Not Est Class 2-Defect Class 3-Defect (3) Class 1-Not Est Class 2-Not Est Class 3-Defect

6.1.5 Interfacial Connections Unsupported holes with leads or PTHs not subjected to mass soldering and used for interfacial connections need not be filled with solder. PTHs not exposed to solder because of permanent or temporary maskant and used for interfacial connections need not be filled with solder.

**6.1.6 Coating Meniscus In Solder** For Class 1 and 2 as an exception to Tables 6-4 or 6-5, as appropriate for supported or unsupported holes, on the solder destination side

the meniscus may be covered by solder but on the solder source side there shall<sup>4</sup> be 360° visible solder wetting and no visible coating meniscus in the solder connection. Solder connections shall<sup>5</sup> meet the requirements of Tables 6-4 or 6-5, as appropriate.

(4) Cla	ss 1-Defect
Cla	ss 2-Defect
Cla	ss 3-Defect
(5) Cla	ss 1-Not Est
	ss 1-Not Est ss 2-Not Est

#### 6.2 Unsupported Holes

#### 6.2.1 Lead Termination Requirements for Unsupported

Holes Lead protrusion for unsupported holes shall<sup>6</sup> meet the requirements of Table 6-2. Solder **shall**<sup>6</sup> meet the requirements of Table 6-4.

(6) Class 1-Defect Class 2-Defect Class 3-Defect

Table 6-4 Unsupported Holes with Component Leads, Minimum Acceptable Conditions<sup>1</sup>

Criteria	Class 1	Class 2	Class 3
Percentage of land area covered with wetted solder <sup>2</sup>	75%	75%	75%
Wetting of lead and land	270°	270°	330°

Note 1. Wetted solder refers to solder applied by the solder process.

Note 2. This applies to any side to which solder was applied.

#### 6.3 Supported Holes

of the PTH.

**6.3.1 Solder Application** Solder shall<sup>7</sup> only be applied to one side of a PTH. Heat may be simultaneously applied to both sides

(7) Class 1-Not Est Class 2-Defect Class 3-Defect

6.3.2 Through-Hole Component Lead Soldering When soldering component leads into PTH connections, the goal of the process is to accomplish 100% fill of the PTH with solder and good wetting top and bottom. The solder con-

nection shall<sup>8</sup> provide evidence of good wetting and the PTH solder fill **shall**<sup>8</sup> meet the requirements of Table 6-5 and Figure 6-2, with solder wetted to the hole wall.

(8) Class 1-Defect Class 2-Defect Class 3-Defect

As an exception to the Class 2 fill requirements in Table 6-5, for plated-through holes connected to thermal or conductor planes that act as thermal heat sinks, a 50% vertical fill of solder is permitted, but with solder extending 360° around the lead with 100% wetting from barrel walls to lead on the secondary side, and the surrounding PTHs meeting requirements of Table 6-5.

Table 6-5	Supported Holes with	Component Leads.	Minimum Acceptable	• Conditions <sup>1</sup>
I able 0-3	Supported Holes With	Component Fears.	. William Acceptable	COHUMICIONS

	Criteria	Class 1	Class 2	Class 3
A.	Circumferential wetting on solder destination side of lead and barrel.	Not specified	180°	270°
B.	Vertical fill of solder. <sup>3,4</sup>	Not specified	75%	75%
C.	Circumferential fillet and wetting on solder source side of lead and barrel. <sup>2</sup>	270°	270°	330 °
D.	Percentage of original land area covered with wetted solder on solder destination side.	0	0	0
E.	Percentage of original land area covered with wetted solder on solder source side. <sup>2</sup>	75%	75%	75%

Note 1. Wetted solder refers to solder applied by any solder process including intrusive soldering.

Note 2. Applies to any side to which solder or solder paste was applied.

Note 3. The 25% unfilled height includes both source and destination side depressions.

Note 4. Class 2 may have less than 75% vertical fill as noted in 6.3.2.

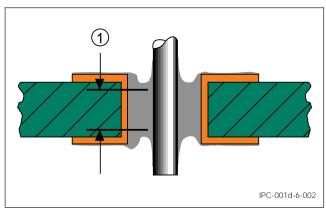


Figure 6-2 Vertical Fill Example

1. Vertical fill

**Note:** Less than 100% solder fill may not be acceptable in some applications (e.g., thermal shock). The user is responsible for identifying these situations to the manufacturer.

#### 7 SURFACE MOUNTING OF COMPONENTS

7.1 Surface Mount Device Lead Forming Leads shall<sup>1</sup> be formed in such a manner that the lead-to-body seal is not damaged or degraded (see Figures 7-1 and 7-2). When lead forming is required during the

assembly process leads **shall** be formed such that there is an available minimum lead length for contact to the solder pad as shown in Table 7-1.

(1) Class 1-Defect Class 2-Defect Class 3-Defect

The leads of surface mounted components **shall**<sup>1</sup> be formed to their final configuration prior to soldering.

**Note:** Where severe loading conditions exist such as Coefficient of Thermal Expansion (CTE) mismatches or severe operational environments, extra consideration should be given to the minimum available contact length.

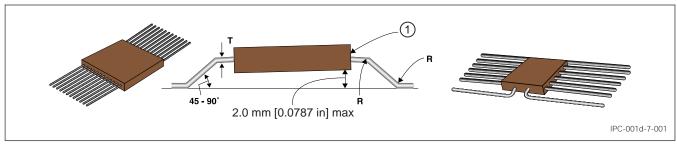


Figure 7-1 Surface Mount Device Lead Forming

1. No bend into the seal

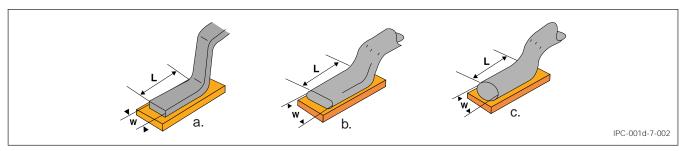


Figure 7-2 Surface Mount Device Lead Forming

Table 7-1 SMT Lead Forming Minimum Lead Length

- A. One lead width for flat leads.
- B. Two lead widths for coined leads.
- C. Two lead diameters for round leads.

7.1.1 Lead Deformation Limits Whether leads are formed manually or by machine or die, parts or components shall not<sup>1</sup> be mounted if the part or component lead has nicks or deformation exceeding 10% of the diameter, width, or thickness of the lead except as allowed for flattened leads (see 7.1.4). Exposed basis metal is acceptable if deformation does not exceed 10% of the diameter, width, or thickness of the lead.

Lead deformation (unintentional bending) may be allowed

- a. There **shall**<sup>1</sup> be no evidence of a short or potential short existing.
- b. The lead-to-body seal or weld **shall not**<sup>1</sup> be damaged by the deformation.
- c. The minimum electrical clearance shall not be violated.
- d. The top of the lead should not extend beyond the top of the component body, except for (1) Class 1-Defect preformed stress loops.
- e. If present on ends, toe curl should not exceed two times the thickness of the lead.

7.1.2 Flat Pack Parallelism Leads on opposite sides of surface mounted flatpacks should be formed such that the nonparallelism between the base surface of the component and the surface of the printed board (i.e., component cant) is minimal. Component cant is permissible, however, the final configuration should not exceed the clearance limit of 2.0 mm [0.0787 in] (see Figure 7-1).

7.1.3 Surface Mount Device Lead Bends Bends shall **not**<sup>2</sup> extend into the seal. (2) Class 1-Defect

The lead-bend radius  $shall^3$  be  $\ge 1T$ where T = nominal lead thickness/diameter (see Figure 7-1).

Class 2-Defect Class 3-Defect (3) Class 1-Accept Class 2-Proc Ind Class 3-Defect

Class 2-Defect

Class 3-Defect

Leads shall<sup>2</sup> be supported during forming to protect the lead-to-body seal.

7.1.4 Flattened Leads Components with axial leads of round cross-section may be flattened (coined) for positive seating in surface mounting. If flattening is used, the flat-

tened thickness shall not4 be less than 40% of the original diameter. Flattened areas of leads are excluded from the 10% deformation requirement of 7.1.1.

(4) Class 1-Not Est Class 2-Not Est Class 3-Defect

7.1.5 Dual-in-Line Packages (DIPs) Dual-in-line packages may be surface mounted provided the leads are configured to meet the mounting requirements for surface mounted leaded parts.

7.1.6 Parts Not Configured for Surface Mounting Components of the through-hole configuration (e.g., transistors, metal power packages, and other nonaxial leaded compo-

nents), shall not<sup>5</sup> be surface mounted unless the leads are formed to meet the surface mount device lead forming requirements.

(5) Class 1-Defect Class 2-Defect Class 3-Defect

7.2 Devices with Externally Deposited Elements Components with electrical elements deposited on an external surface (such as chip resistors) shall<sup>6</sup>

be mounted with that surface away from the printed board or substrate.

(6) Class 1-Not Est Class 2-Proc Ind Class 3-Proc Ind

7.3 Leaded Component Body Clearing The maximum clearance between the bottom of a leaded component body and the printed circuit surface should be 2 mm [0.078 in]. Parts insulated from circuitry or over surfaces without exposed circuitry may be mounted flush. Uninsulated parts

mounted over exposed circuitry shall<sup>7</sup> have their leads formed to provide a minimum of 0.25 mm [0.00984 in] between the bottom of the component body and the exposed circuitry.

(7) Class 1-Not Est Class 2-Not Est Class 3-Defect

- 7.3.1 Axial-Leaded Components The body of a surface mounted axial-leaded component should not be spaced above the surface of the printed board more than 2 mm [0.078 in], unless the component is mechanically attached to the substrate by adhesive or other mechanical means (see Figure 7-1).
- 7.4 Parts Configured for Butt Lead Mounting Parts may be configured for surface butt mounting on Class 1 and 2 products. Components designed for pin-in-hole application and modified for butt connection attachment, or stiff-leaded dual-in-line packages (e.g., alloy 42,

brazed or tempered leads, etc.) may be butt mounted. Butt mounting shall **not**<sup>8</sup> be permitted on Class 3 products. (8) Class 1-Not Est Class 2-Not Est Class 3-Defect

7.5 Hold Down of Surface Mount Leads Surface mounted device leads shall not<sup>9</sup> be held down under stress (e.g., by probes) during solder solidification such that the resulting residual stresses remain.

The resistance reflow system shall **not**<sup>9</sup> deflect the leads more than two times the lead thickness during reflow.

(9) Class 1-Not Est Class 2-Not Est Class 3-Defect

**7.6 Soldering Requirements** Solder connections or terminations on components designed for surface mounting **shall**<sup>1</sup> exhibit conditions that meet the general descriptions

of 4.14, and **shall not**<sup>1</sup> exhibit any of the defect conditions of 4.14.3, with the specific dimensions defined in 7.6.3 through 7.6.16 (see Table 7-2).

(1) Class 1-Defect Class 2-Defect Class 3-Defect

**7.6.1 Misaligned Components** Some surface mounted components will self-align during reflow soldering but a

degree of misalignment is permitted to the extent specified in Tables 7-3 through 7-16; however, minimum design electrical clearance **shall not**<sup>2</sup> be violated.

(2) Class 1-Defect Class 2-Defect Class 3-Defect

**7.6.2 Unspecified and Special Requirements** Some dimensions, e.g., solder thickness, are not inspectable conditions and are identified by notes.

Dimension (G) is the solder fillet from the top of the land to the bottom of the termination. Dimension (G) is the prime parameter in the determination of solder connection reliability for leadless components. A thick (G) is desirable.

Additional information related to reliability of surface mount connections is available in IPC-D-279, IPC-SM-785 and IPC-9701.

Table 7-2 Surface Mount Components

Bottom Only Terminations	7.6.3
Rectangular or Square End Component Termination	7.6.4
Cylindrical End Cap Terminations (MELF)	7.6.5
Castellated Terminations	7.6.6
Flat, Ribbon, "L," and Gull Wing Lead Terminations	7.6.7
Round or Flattened (Coined) Lead Terminations	7.6.8
"J" Lead Terminations	7.6.9
Butt Connection Terminations	7.6.10
Flat Lug Lead Terminations	7.6.11
Tall Profile Components Having Bottom Only Terminations	7.6.12
Inward Formed L-shaped Ribbon Lead Terminations	7.6.13
Surface Mount Area Array Packages	7.6.14
Quad Flat Pack-No Leads QFN	7.6.15
Bottom Thermal Plane Terminations	7.6.16

**7.6.3 Bottom Only Terminations** Discrete chip components, leadless chip carriers, and other devices having metallized terminations on the bottom side only (except ball grid arrays) **shall**<sup>1</sup> meet the dimensional and solder fillet requirements of Table 7-3 and Figure 7-3 for each product classification. The widths of the component and land are W and P, respectively, and the termination overhang describes the condition whereby the smaller extends beyond the larger termination (i.e., W or P).

Table 7-3 Dimensional Criteria - Bottom Only Terminations

Feature	Dim.	Class 1	Class 2	Class 3
Maximum Side Overhang	А	50% (W) or 50% (P), whichever is less; Note 1		25% (W) or 25% (P), whichever is less; Note 1
End Overhang	В		Not permitted	
Minimum End Joint Width	С	50% (W) or 50% (P), whichever is less		75% (W) or 75% (P), whichever is less
Minimum Side Joint Length	D	Note 3		
Maximum Fillet Height	E	Note 3		
Minimum Fillet Height	F	Note 3		
Solder Thickness	G	Note 3		
Minimum End Overlap	J	Required		
Termination Length	L	Note 2		
Land Width	Р	Note 2		
Termination Width	W	Note 2		

- Note 1. Does not violate minimum electrical clearance.
- Note 2. Unspecified parameter or variable in size, determined by design.
- Note 3. Wetting is evident.

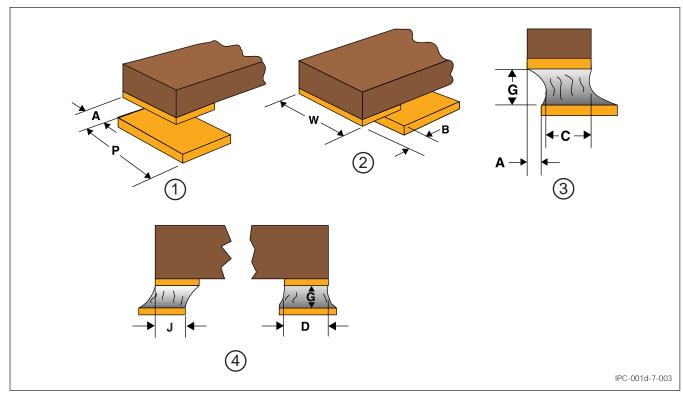


Figure 7-3 Bottom Only Terminations

- 1. Side overhang
- 2. End overhang
- 3. End joint width
- 4. Side joint length, end overlap

#### 7.6.4 Chip Components - Rectangular or Square End Components - 1, 3 or 5 Side Termination

These criteria apply to component types such as Chip Resistor, Chip Capacitor, and Square End MELF.

Solder connections to components having terminations of a square or rectangular configuration shall<sup>1</sup> meet the dimensional and solder fillet requirements of Table 7-4 and Figure 7-4 for each product classification. For 1 sided termination, the solderable side is the vertical end face of the component.

Table 7-4 Dimensional Criteria - Chip Components - Rectangular or Square End Components - 1, 3 or 5 Side Termination

Feature	Dim.	Class 1	Class 2	Class 3	
Maximum Side Overhang	А	50% (W) or 50% (P), whichever is less; Note 1		25% (W) or 25% (P), whichever is less; Note 1	
End Overhang	В		Not pe	rmitted	
Minimum End Joint Width	С		or 50% (P), less; Note 5	75% (W) or 75% (P), whichever is less; Note 5	
Minimum Side Joint Length	D		No	te 3	
Maximum Fillet Height	E		No	te 4	
Minimum Fillet Height	F		the vertical surface(s) termination. Note 6	(G) + 25% (H) or (G) + 0.5 mm [0.02 in], whichever is less. Note 6	
Solder Thickness	G		No	te 3	
Termination Height	Н	Note 2			
Minimum End Overlap	J	Required			
Width of Land	Р	Note 2			
Termination Width	W	Note 2			
		Side Mounting	/Billboarding, Notes 7,	8	
Width to Height Ratio			Does not	exceed 2:1	
End Cap and Land Wetting		10	0% wetting land to end	metallization contact areas	
Minimum End Overlap	J	100%			
Maximum Side Overhang	Α	Not permitted			
End Overhang	В	Not permitted			
Maximum Component Size		No limits 1206			
Termination Faces		Three or more faces			

- Note 1. Does not violate minimum electrical clearance.
- Note 2. Unspecified parameter or variable in size as determined by design.
- Note 3. Wetting is evident.
- Note 4. The maximum fillet may overhang the land and/or extend onto the top of the end cap metallization; however, the solder does not extend further onto the top of the component body.
- Note 5: (C) is measured from the narrowest side point of the solder fillet.
- Note 6: Designs with via in pad may preclude meeting these criteria. Solder acceptance criteria should be defined between the user and the manufacturer.
- Note 7: These criteria are for chip components that may flip (rotate) onto the narrow edge during assembly.
- Note 8: These criteria may not be acceptable for certain high frequency or high vibration applications.

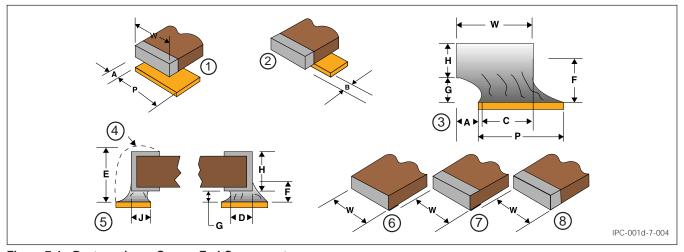


Figure 7-4 Rectangular or Square End Components

- 1. Side overhang
- 2. End overhang
- 3. End joint width
- 4. See Note 4, Table 7-4
- 5. Side joint length, end overlap
- 6. One or two face termination
- 7. Three face termination
- 8. Five face termination

**7.6.5 Cylindrical End Cap (MELF) Terminations** Solder connections to components having cylindrical end cap terminations **shall**<sup>1</sup> meet the dimensional and solder fillet requirements of Table 7-5 and Figure 7-5 for each product classification.

Table 7-5 Dimensional Criteria - Cylindrical End Cap (MELF) Terminations

Feature	Dim.	Class 1	Class 2	Class 3	
Maximum Side Overhang	А	25% (W) or 25% (P), whichever is less; Note 1			
End Overhang	В		Not permitted		
Minimum End Joint Width, Note 2	С	Note 4	50% (W) or 50% (P	), whichever is less	
Minimum Side Joint Length	D	Notes 4, 6 50% (R) or 50% (S), whichever is less; Note 6		75% (R) or 75% (S), whichever is less; Note 6	
Maximum Fillet Height	Е	Note 5			
Minimum Fillet Height (end and side)	F	Wetting is evident on the vertical surface(s) (G) + 25% (W) or (G) + 1.0 mm [0.0394 in whichever is less. Note			
Solder Thickness	G		Note 4		
Minimum End Overlap	J	Notes 4, 6	50% (R) Note 6	75% (R) Note 6	
Land Width	Р	Note 3			
Termination/Plating Length	R	Note 3			
Land Length	S	Note 3			
Termination Diameter	W	Note 3			

- Note 1. Does not violate minimum electrical clearance.
- Note 2. (C) is measured from the narrowest point of the solder fillet.
- Note 3. Unspecified parameter or variable in size as determined by design.
- Note 4. Wetting is evident.
- Note 5. The maximum fillet may overhang the land or extend onto the top of the component termination; however, the solder does not extend further onto the component body.
- Note 6. Does not apply to components with end-only terminations.
- Note 7: Designs with via in pad may preclude meeting these criteria. Solder acceptance criteria should be defined between the user and the manufacturer.

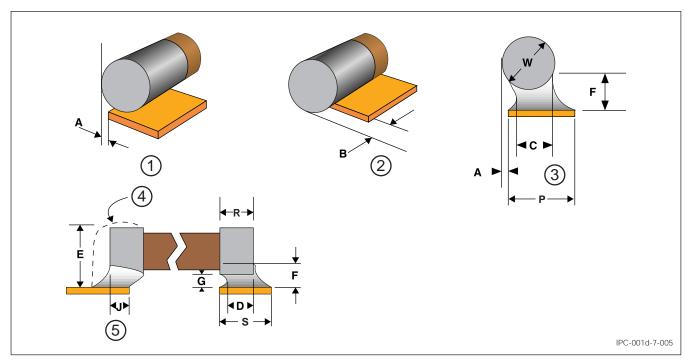


Figure 7-5 MELF Terminations

- 1. Side overhang
- 2. End overhang
- 4. See Note 4, Table 7-5
- 5. Side joint length and end overlap
- 3. End joint width

**7.6.6 Castellated Terminations** Connections formed to castellated terminations **shall**<sup>1</sup> meet the dimensional and solder fillet requirements of Table 7-6 and Figure 7-6 for each product classification.

Table 7-6 Dimensional Criteria - Castellated Terminations

Feature	Dim.	Class 1	Class 2	Class 3
Maximum Side Overhang	Α	50% (W) Note 1		25% (W) Note 1
End Overhang	В	Not permitted		
Minimum End Joint Width	С	50% (W)		75% (W)
Minimum Side Joint Length, Note 4	D	Note 3	3 Depth of castellation	
Maximum Fillet Height	Е	G + H		
Minimum Fillet Height	F	Note 3	(G) + 25% (H)	(G) + 50% (H)
Solder Thickness	G	Note 3		
Castellation Height	Н	Note 2		
Land Length	S	Note 2		
Castellation Width	W	Note 2		

- Note 1. Does not violate minimum electrical clearance.
- Note 2. Unspecified parameter or variable in size as determined by design.
- Note 3. Wetting is evident.
- Note 4. Length "D" is dependent upon fillet height "F."

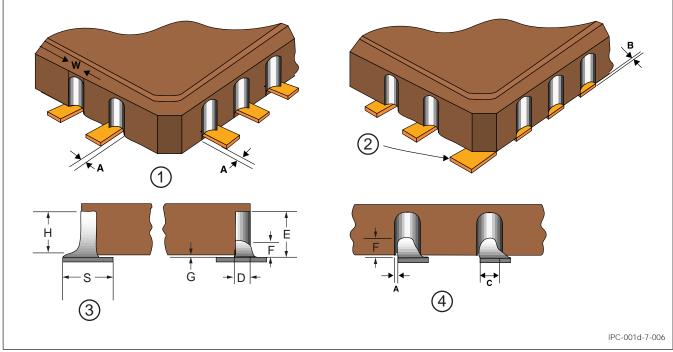


Figure 7-6 Castellated Terminations

- 1. Side overhang
- 2. Corner (termination) fillet required if metallization is present
- 3. Side joint length
- 4. Side overhang/end joint width

**7.6.7 Flat, Ribbon, "L," and Gull Wing Leads** Connections formed to flat, ribbon, "L," and gull wing shaped leads of either stiff or flexible materials **shall**<sup>1</sup> meet the alignment and solder fillet requirements of Table 7-7 and Figure 7-7 for each product classification.

(1) Class 1-Defect Class 2-Defect Class 3-Defect

In the following criteria, the words "plastic component" are used in the generic sense to differentiate between plastic components and those made of other materials, e.g., ceramic/alumina or metal (normally hermetically sealed).

Table 7-7 Dimensional Criteria - Flat, Ribbon, "L," and Gull Wing Leads

Fea	Feature Dim.		Class 1	Class 2	Class 3		
Maximum Side Overhang		А	50% (W) or 0.5 mm [0.02 in], whichever is less; Note 1		25% (W) or 0.5 mm [0.02 in], whichever is less; Note 1		
Maximum Toe Overhang		В	Note 1				
Minimum End Joint Width		С	50% (W)		75% (W)		
	D	(1W) or 0.5 mm [0.02 in],	3 (W) or 75% (L), whichever is longer				
		D	whichever is less	100% (L)			
Maximum Heel Fillet Height		Е	Note 4				
Minimum Heel Fillet Height		F	Note 3	(G) + 50% (T) Note 5	(G) + (T) Note 5		
Solder Thickness		G	Note 3				
Formed Foot Length		L	Note 2				
Lead Thickness		Т	Note 2				
Lead Width		W	Note 2				

- Note 1. Does not violate minimum electrical clearance.
- Note 2. Unspecified parameter or variable in size as determined by design.
- Note 3. Wetting is evident.
- Note 4. Solder fillet may extend through the top bend. Solder does not touch package body or end seal, except for plastic SOIC or SOT devices. Solder should not extend under the body of surface mount components whose leads are made of Alloy 42 or similar metals.
- Note 5. In the case of a toe-down lead configuration, the minimum heel fillet height (F) extends at least to the mid-point of the outside lead bend.
- Note 6. Fine pitch leads require a minimum side fillet length of 0.5 mm [0.02 in].

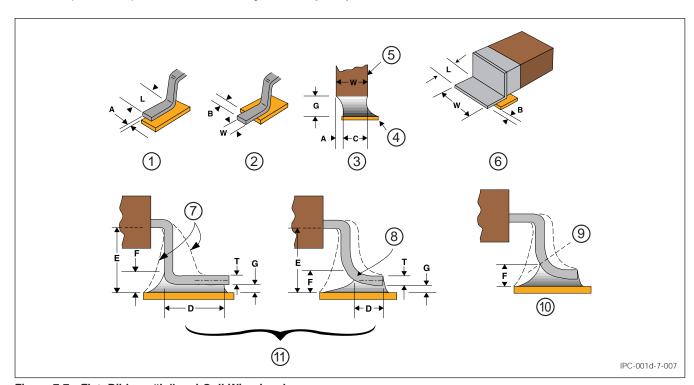


Figure 7-7 Flat, Ribbon, "L," and Gull Wing Leads

- 1. Side overhang
- 2. Toe overhang
- 3. End joint width
- 4. Land
- 5. Lead6. Other lead configurations
- 7. See Note 4, Table 7-7
- 8. Center line of (T)
- 9. Line bisecting lower bend
- 10. Toe down heel fillet height
- 11. Side joint length

**7.6.8 Round or Flattened (Coined) Leads** Connections formed to round or flattened (coined) leads **shall<sup>1</sup>** meet the dimensional and fillet requirements of Table 7-8 and Figure 7-8 for each product classification.

Table 7-8 Dimensional Criteria - Round or Flattened (Coined) Leads

Feature	Dim.	Class 1	Class 2	Class 3
Maximum Side Overhang	А	50% (W) or 0.5 mm [0.02 in], whichever is less; Note 1		25% (W) or 0.5 mm [0.02 in], whichever is less; Note 1
Maximum Toe Overhang	В	Note 1		
Minimum End Joint Width	С	Note 3		75% (W)
Minimum Side Joint Length	D	100% (W)		150% (W)
Maximum Heel Fillet Height	Е	Note 4		
Minimum Heel Fillet Height	F	Note 3	(G) + 50% (T) Note 5	(G) + (T) Note 5
Solder Thickness	G	Note 3		
Formed Foot Length	L	Note 2		
Minimum Side Joint Height	Q	Note 3 (G) + 50% (T)		50% (T)
Thickness of Lead at Joint Side	Т	Note 2		
Flattened Lead Width or Diameter of Round Lead	W	Note 2		

- Note 1. Does not violate minimum electrical clearance.
- Note 2. Unspecified parameter or variable in size as determined by design.
- Note 3. Wetting is evident.
- Note 4. Solder fillet may extend through the top bend. Solder does not touch package body or end seal, except for plastic SOIC or SOT devices. Solder should not extend under the body of surface mount components whose leads are made of Alloy 42 or similar metals.
- Note 5. In the case of a toe-down lead configuration, the minimum heel fillet height (F) extends at least to the mid-point of the outside lead bend.

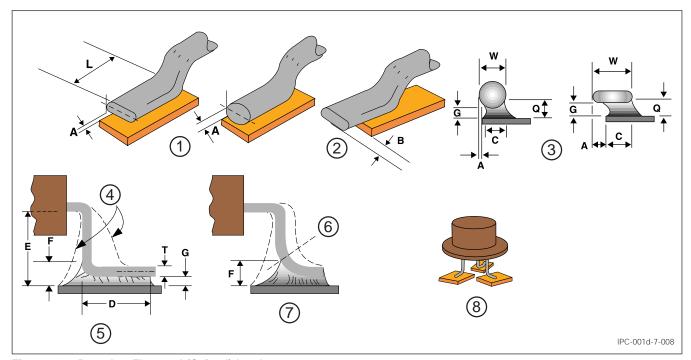


Figure 7-8 Round or Flattened (Coined) Leads

- 1. Side overhang
- 2. Toe overhang
- 3. End joint width
- 4. See Note 4, Table 7-8
- 5. Side joint length
- 6. Line bisecting lower bend
- 7. Toe down heel fillet height
- 8. Other land configurations

**7.6.9** "J" Leads Connections formed to leads having a "J" shape at the connection site shall meet the dimensional and fillet requirements of Table 7-9 and Figure 7-9 for each product classification.

Table 7-9 Dimensional Criteria - "J" Leads

Feature	Dim.	Class I	Class 2	Class 3
Maximum Side Overhang	A	50% (W	) Note 1	25% (W) Note 1
Maximum Toe Overhang	В		Notes 1, 2	
Minimum End Joint Width	С	50%	(W)	75% (W)
Minimum Side Joint Length	D	Note 3	1	50% (W)
Maximum Fillet Height	E	Note 4		
Minimum Heel Fillet Height	F	(G) + 50% (T) (G) + (		(G) + (T)
Solder Thickness	G	Note 3		
Lead Thickness	Т	Note 2		
Lead Width	W	Note 2		

- Note 1. Does not violate minimum electrical clearance.
- Note 2. Unspecified parameter or variable in size as determined by design.
- Note 3. Wetting is evident.
- Note 4. Solder fillet does not touch package body.

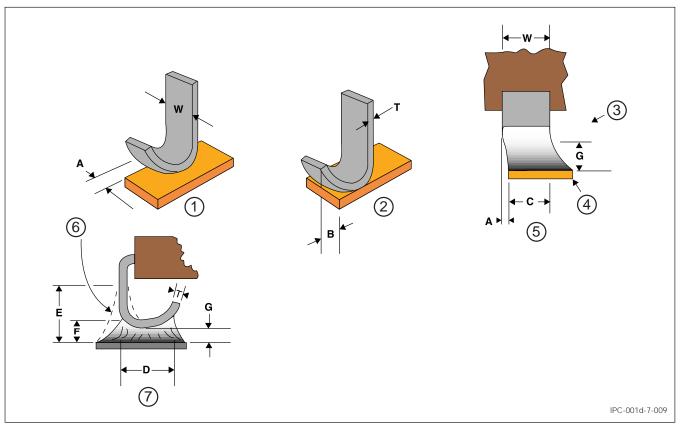


Figure 7-9 "J" Leads

- 1. Side overhang
- 2. Toe overhang
- 3. Lead
- 4. Land

- 5. End joint width
- 6. See Note 4, Table 7-9
- 7. Side joint length

**7.6.10 Butt Connections (Not Permitted for Class 3 Products)** Connections formed to leads positioned perpendicular to a circuit land in a butt configuration **shall**<sup>1</sup> meet the dimensional and solder fillet requirements of Table 7-10 and Figure 7-10 for each product classification.

(1) Class 1-Defect Class 2-Defect Class 3-Defect

Table 7-10 Dimensional Criteria - Butt/I Connections (Not Applicable to Class 3)

Feature	Dim.	Class 1	Class 2
Maximum Side Overhang	А	25% (W) Note 1 Not permitted	
Maximum Toe Overhang	В	Not pe	rmitted
Minimum End Joint Width	С	75%	, (W)
Minimum Side Joint Length	D	Note 2	
Maximum Fillet Height	Е	Note 4	
Minimum Fillet Height	F	0.5 mm [0.0197 in]	
Solder Thickness	G	Note 3	
Lead Thickness	Т	Note 2	
Lead Width	W	Note 2	

Note 1. Does not violate minimum electrical clearance.

Note 2. Unspecified parameter or variable in size as determined by design.

Note 3. Wetting is evident.

Note 4. Maximum fillet may extend into the bend radius. Solder does not touch package body.

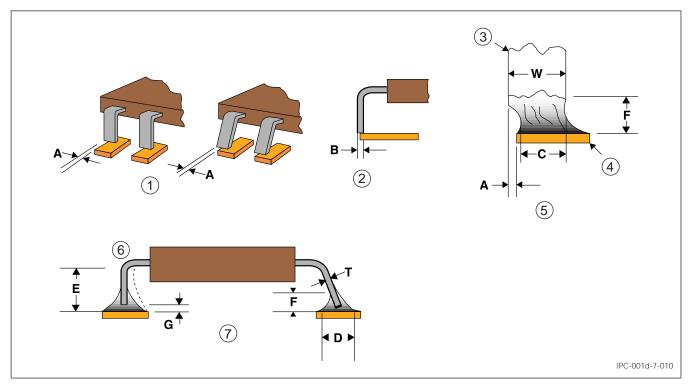


Figure 7-10 Butt Joint

- 1. Side overhang
- 2. Toe overhang
- 3. Lead
- 4. Land

- 5. End joint width
- 6. See Note 4, Table 7-10
- 7. Side joint length

**7.6.11 Flat Lug Leads** Connections formed to the leads of power dissipating components with flat lug lead **shall**<sup>1</sup> meet the dimensional requirements of Table 7-11 and Figure 7-11.

Table 7-11 Dimensional Criteria - Flat Lug Leads

Feature	Dim.	Class 1	Class 2	Class 3
Maximum Side Overhang	Α	50% (W) Note 1	25% (W) Note 1	Not permitted
Maximum Toe Overhang	В	Note 1	Not p	ermitted
Minimum End Joint Width	С	50% (W)	75% (W)	(W)
Minimum Side Joint Length	D	Note 3	(L)-(M	), Note 4
Maximum Fillet Height	Е	Not	te 2	(G) + (T) + 1.0 mm [0.039 in]
Minimum Fillet Height	F	Note 3		(G) + (T)
Solder Fillet Thickness	G	Note 3		
Lead Length	L	Note 2		
Maximum Gap	М		Note 2	
Land Width	Р	Note 2		
Lead Thickness	Т	Note 2		
Lead Width	W	Note 2		

- Note 1. Does not violate minimum electrical clearance.
- Note 2. Unspecified parameter or variable in size as determined by design.
- Note 3. Wetting is evident.
- Note 4. Where the lug is intended to be soldered beneath the component body and the land is designed for the purpose, the lead shows evidence of wetting in the gap M.

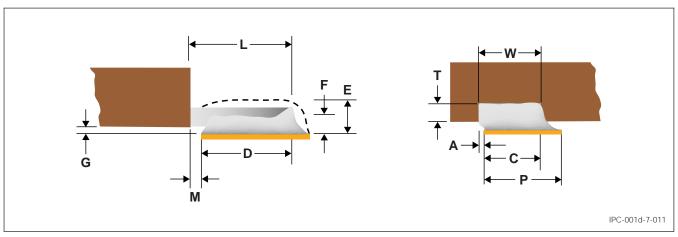


Figure 7-11 Flat Lug Leads

**7.6.12 Tall Profile Components Having Bottom Only Terminations** Connections formed to the termination areas of tall profile components (component height is more than twice the component width or thickness, whichever is less) having bottom only terminations **shall**<sup>1</sup> meet the dimensional requirements of Table 7-12 and Figure 7-12. If the height of the component exceeds the thickness of the component, it should not be used in products subject to vibration and/or shock unless an appropriate adhesive is used to reinforce the component mounting.

Table 7-12 Dimensional Criteria - Tall Profile Components Having Bottom Only Terminations

Feature	Dim.	Class 1	Class 2	Class 3
Maximum Side Overhang	А	50% (W); Notes 1, 4	25% (W); Notes 1, 4	Not permitted; Notes 1, 4
Maximum End Overhang	В	Notes 1, 4	Not pe	ermitted
Minimum End Joint Width	С	50% (W)	75% (W)	(W)
Minimum Side Joint Length	D	Note 3	50% (S)	75% (S)
Solder Fillet Thickness	G		Note 3	
Land Length	S	Note 2		
Termination Width	W	Note 2		

- Note 1. Does not violate minimum electrical clearance.
- Note 2. Unspecified parameter or variable in size as determined by design.
- Note 3. Wetting is evident.
- Note 4. As a function of the component design, the termination may not extend to the component edge, and the component body may overhang the PCB land area. The component solderable termination area does not overhang PCB land area.

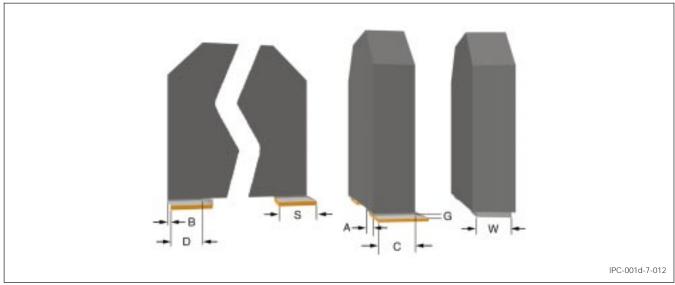


Figure 7-12 Tall Profile Components Having Bottom Only Terminations

**7.6.13 Inward Formed L-Shaped Ribbon Leads** Connections formed to components having Inward Formed L-shaped lead terminations **shall**<sup>1</sup> meet the dimensional and solder fillet requirements of Table 7-13 and Figure 7-13.

Table 7-13 Dimensional Criteria - Inward Formed L-Shaped Ribbon Leads<sup>5</sup>

Feature	Dim.	Class 1	Class 2	Class 3	
Maximum Side Overhang	А	50% (W) Notes 1, 5		25% (W) or 25% (P), whichever is less; Notes 1, 5	
Maximum Toe Overhang	В	Note 1	Not Pe	ermitted	
Minimum End Joint Width	O	50%	5 (W)	75% (W) or 75% (P), whichever is less	
Minimum Side Joint Length	D	Note 3	50% (L)	75% (L)	
Maximum Fillet Height	Е	(H) + (G) Note 4	(H) + (G) Note 4	(H) + (G) Note 4	
Minimum Fillet Height, Notes 5, 6	F	Wetting is evident on the vertical surface(s) of the component termination (G) + 25% (H) or (G) + whichever			
Solder Fillet Thickness	G	Note 3			
Lead Height	Н		Note 2		
Minimum Land Extension	K	Note 2			
Lead Length	L	Note 2			
Land Width	Р	Note 2			
Land Length	S	Note 2			
Lead Width	W	Note 2			

- Note 1. Does not violate minimum electrical clearance.
- Note 2. Unspecified parameter or variable in size as determined by design.
- Note 3. Wetting is evident.
- Note 4. Solder does not contact the component body on the inside of the lead bend.
- Note 5. Where a lead has two prongs, the connection to each prong is to meet all the specified requirements.
- Note 6. Designs with via in pad may preclude meeting these criteria. Solder acceptance criteria should be defined between the user and the manufacturer.

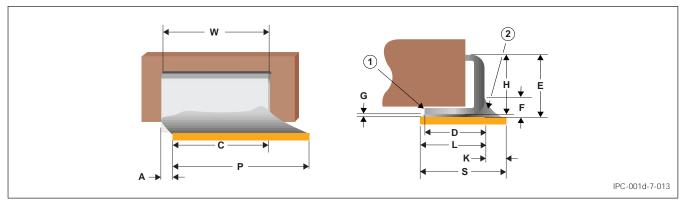


Figure 7-13 Inward Formed L-Shaped Ribbon Lead

- 1. Toe
- 2. Heel

**7.6.14 Surface Mount Area Array Packages** These criteria are intended to apply to devices with solder balls that collapse during reflow.

A BGA criterion defined herein assumes an inspection process is established to determine compliance for either X-Ray or normal visual inspection processes. To a limited extent, this may involve visual assessment, but more commonly requires evaluation of X-Ray images to allow assessment of characteristics that cannot be accomplished by normal visual means.

Visual inspection requirements:

- When visual inspection is the method used to verify product acceptance the magnification levels of Tables 11-1 and 11-2 apply.
- The solder terminations on the outside row (perimeter) of the BGA should be visually inspected whenever practical.
- The BGA needs to align in both X & Y directions with the corner markers on the PCB (if present).
- Absence of BGA solder ball(s) are defects unless specified by design.

Process development and control is essential for continued success of assembly methods and implementation of materials. Process validation and control can be used in lieu of X-ray/visual inspection provided objective evidence of compliance is available.

BGA process guidance is provided in IPC-7095, which contains recommendations developed from extensive discussion of BGA process development issues.

**Note:** X-ray equipment not intended for electronic assemblies or not properly set up can damage sensitive components.

Surface mount area array packages **shall**<sup>1</sup> meet the dimensional and solder fillet requirements of Table 7-14.

(1) Class 1-Defect Class 2-Defect Class 3-Defect

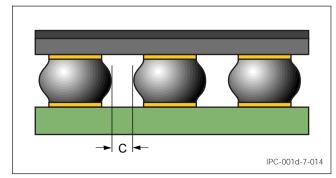


Figure 7-14 BGA Solder Ball Spacing

Table 7-14 Dimensional Criteria - Area Array/Ball Grid Array

Feature	Classes 1,2,3
Alignment	Solder ball offset does not violate minimum electrical clearance.
Solder Ball Spacing, Figure 7-14	Solder ball offset (c) does not violate minimum electrical clearance.
Soldered Connection	<ul><li>a. Solder connections meet the criteria of 4.14.</li><li>b. BGA solder balls contact and wet to the land forming a continuous elliptical round or pillar connection.</li></ul>
Voids	25% or less voiding of the ball x-ray image area. Notes 1, 2.
Under-fill or staking material	Required underfill or staking material is present and completely cured.

Note 1. Design induced voids, e.g., microvia in land, are excluded from this criteria. In such cases acceptance criteria will need to be established between the manufacturer and user.

Note 2. Manufacturers may use test or analysis to develop alternate acceptance criteria for voiding that consider the end-use environment.

**7.6.15** Quad Flat Pack (No Leads) (QFNL) These criteria are also applicable to Small Outline Integrated Circuit (No Leads) [SOICNL].

Criteria for nonvisible part of thermal plane solder connections are not described in this document and will need to be established by agreement between the user and the manufacturer. The thermal transfer plane acceptance criteria are design and process related. Issues to consider include but are not limited to component manufacturer's application notes, solder coverage, voids, solder height, etc. When soldering these types of components voiding in the

thermal plane is common. Solder, when required, **shall**<sup>1</sup> meet documented requirements.

Connections formed to components having no significant external lead form **shall**<sup>1</sup> meet the dimensional and solder fillet requirements of Table 7-15 and Figure 7-15.

There are some package configurations that have no toe exposed or do not have a continuous solderable surface on the exposed toe on the exterior

(1) Class 1-Defect Class 2-Defect Class 3-Defect

of the package and a toe fillet will not form.

Table 7-15 Dimensional Criteria - PQFN

Feature	Dim.	Class 1	Class 2	Class 3
Maximum Side Overhang	Α	50% W, Note 1	25% W	/, Note 1
Toe Overhang (outside edge of component termination)	В	Not Permitted		
Minimum End Joint Width	С	50% W	759	% W
Minimum Side Joint Length	D		Note 4	
Solder Fillet Thickness	G	Note 3		
Minimum Toe (End) Fillet Height	F	Notes 2, 5		
Termination Height	Н	Note 5		
Solder coverage of thermal pad		Note 4		
Land Width	Р	Note 2		
Termination Width	W	Note 2		

- Note 1. Does not violate minimum electrical clearance.
- Note 2. Unspecified parameter or variable in size as determined by design.
- Note 3. Wetting is evident.
- Note 4. Not a visually inspectable attribute.

Note 5. "H" = height of solderable surface of lead, if present. Some package configurations do not have a continuous solderable surface on the sides and do not require a toe (end) fillet.

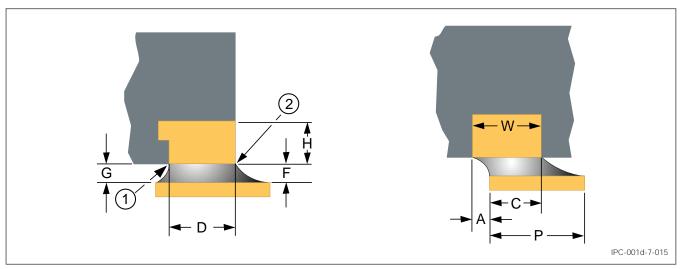


Figure 7-15 PQFN

**7.6.16** Components with Bottom Thermal Plane Terminations Criteria for the nonvisible part of components such as D-Pak<sup>TM</sup> with nonvisible connections are not described in this document and will need to be established by agreement between the user and the manufacturer. The thermal transfer plane acceptance criteria are design and process related. Issues to consider include but are not limited to component manufacturer's application notes, solder coverage, voids, solder height, etc. Solder, when required, **shall** meet documented requirements. When soldering these types of components voiding in the thermal plane is common.

**Note:** The criteria for leads other than the thermal plane termination are provided in 7.6.7.

Connections formed to components with bottom thermal plane terminations **shall**<sup>1</sup> meet the dimensional and solder fillet requirements of Table 7-16.

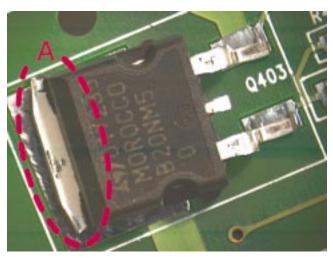


Figure 7-16 Component with Bottom Thermal Plane Termination

Table 7-16 Dimensional Criteria - Bottom Thermal Plane Terminations

Feature (all connections except thermal plane)	Dim.	
Maximum Side Overhang	А	
Toe Overhang (outside edge of component termination)	В	
Minimum End Joint Width	С	Can 7.0.7
Minimum Side Joint Length	D	See 7.6.7
Maximum Heel Fillet Height	E	
Minimum Heel Fillet Height	F	
Solder Fillet Thickness	G	
Feature (only for the thermal plane connection)		Class 1,2,3
Thermal Plane Side Overhang (Figure 7-16)		Not greater than 25% of termination width.
Thermal Plane End Overhang		No overhang.
Thermal Plane End Joint Width		100% wetting to land in the end-joint contact area.

### **8 CLEANING PROCESS REQUIREMENTS**

An item that is required to be cleaned **shall**<sup>1</sup> be cleaned per a documented process to allow removal of all contaminants (especially flux residue). The items cleaned **shall**<sup>2</sup> be capable of meeting the cleanliness requirement as specified herein (see 8.3).

All items to be cleaned **shall**<sup>2</sup> be cleaned in a manner that will prevent thermal shock and/or detrimental intrusion of cleaning media into components that are not totally sealed.

(1) Class 1-Not Est Class 2-Not Est Class 3-Defect

(2) Class 1-Not Est Class 2-Defect Class 3-Defect

**8.1 Cleanliness Exemptions** Terminations internal to self-sealing devices (e.g., heat shrinkable solder devices) are exempt from the cleaning requirements of this standard when the device encapsulates the solder connection.

- **8.2 Ultrasonic Cleaning** Ultrasonic cleaning is permissible:
- a. On bare boards or assemblies, provided only terminals or connectors without internal electronics are present.
- b. On electronic assemblies with electrical components, provided the manufacturer has documentation available for review showing that the use of ultrasonics does not damage the mechanical or electrical performance of the product or components being cleaned, see IPC-TM-650 test methods 2.6.9.1 Test to Determine Sensitivity of Electronic Assemblies to Ultrasonic Energy and 2.6.9.2 Test to Determine Sensitivity of Electronic Components to Ultrasonic Energy.
- **8.3 Post-Solder Cleanliness** Visual inspection is used to assess the presence of foreign particulate matter as required in 8.3.1, or flux and other ionic or organic residues as required in 8.3.2 (see 11.2.2).
- **8.3.1 Particulate Matter** Assemblies **shall**<sup>3</sup> be free of dirt, lint, solder splash, webbing, dross, wire clippings, etc. Solder balls **shall**<sup>3</sup> neither be loose (i.e., be dislodged in the normal ser-

Class 2-Defect Class 3-Defect

### 8.3.2 Flux Residues and Other Ionic or Organic Con-

taminants Unless specified by the user, the manufacturer should specify a cleanliness designator that establishes the cleaning option and test for cleanliness in accordance with 8.3.3 and in compliance with 3, Materials, Components and Equipment Requirements. In the absence of a specified

cleanliness designator, the designator C-22 as described in the following paragraphs and the visual requirements for cleanliness **shall**<sup>4</sup> apply.

vice environment of the product) nor

violate minimum electrical clearance.

(4) Class 1-Defect Class 2-Defect Class 3-Defect **Note:** This requirement may be eliminated when visible residue has been identified as benign through laboratory analysis or other means.

**8.3.3 Post-Soldering Cleanliness Designator** The cleanliness designator is to be in the following form: A 2-digit (minimum) code describes the cleanliness requirements for all assemblies covered under this standard. This code begins with the letter "C" then a dash followed by two or more digits. The first digit represents the cleaning option described in 8.3.4 and the second and following digits indicate the requirements for cleanliness testing described in 8.3.5.

**8.3.4 Cleaning Option** The first digit of the cleanliness designator defines the cleaning option. The digits in Table 8-1 are used to define the surfaces of the assembly that are to be cleaned.

Table 8-1 Designation of Surfaces to be Cleaned

0	No surfaces to be cleaned
1	One side (solder source side) of assembly to be cleaned
2	Both sides of assembly to be cleaned

**8.3.5 Test for Cleanliness** The second and following digits of the cleanliness designator define the requirements for cleanliness testing. The digits in Table 8-2 apply.

Table 8-2 Cleanliness Testing Designators

0	No test for cleanliness required
1	Test for rosin residues required (8.3.6.1)
2	Test for ionic residues required (8.3.6.2 and/or 8.3.6.3)
3	Test for surface insulation resistance (8.3.6.4)
4	Test for other surface organic contaminants (8.3.6.5)
5	Other tests as defined by user/manufacturer agreement

**8.3.6 Testing** If required, periodic testing of cleanliness of the printed circuit assemblies after final cleaning (e.g., the cleaning prior to conformal coating, encapsulation, or incorporation into the next higher assembly) **shall**<sup>5</sup> be conducted on a random sample basis (see 11.2.3) to ensure the adequacy of the cleaning process(es). If any printed circuit

assembly fails, the entire lot **shall**<sup>5</sup> be evaluated and recleaned if necessary and a random sample of this lot and each lot cleaned since performing the last acceptable cleanliness test **shall**<sup>5</sup> be tested.

(5) Class 1-Defect Class 2-Defect Class 3-Defect

(6) Class 1-Not Est Class 2-Proc Ind Class 3-Defect

The frequency of testing **shall**<sup>6</sup> be a minimum of once each production shift unless the process control system data supports a change in frequency.

8.3.6.1 Rosin Flux Residues When rosin flux residue testing is required, assemblies shall<sup>1</sup> be tested in accordance with IPC-TM-650, Test Method 2.3.27 and shall<sup>1</sup> comply with the following requirements for the maximum allowable level of flux residues:

(1) Class 1-Defect Class 2-Defect Class 3-Defect

Class 1 assemblies less than 200 micrograms/cm<sup>2</sup> Class 2 assemblies less than 100 micrograms/cm<sup>2</sup>

Class 3 assemblies less than 40 micrograms/cm<sup>2</sup>

8.3.6.2 Ionic Residues (Instrument Method) When ionic residue (instrument method) testing is required, assemblies shall<sup>2</sup> be tested in accordance with IPC-TM-650, Method 2.3.25C, Detection and Measurement of Ionizable Surface Contaminants. Dynamic Extraction Methods should be performed in compliance with Test Method 2.3.25, item 5. Static Extraction Methods should be performed in compliance with Test Method 2.3.25, item 6.

Other methods may be used when the sensitivity of the alternative method is shown to be equal to or better than the above methods with respect to detecting ionizable surface contamination. In comparing the sensitivity between methods, the solvent used to extract the residue, the method used to present the solvent to the assembly, and the method of detecting the residue should all be considered.

For assemblies soldered with ROL0 or ROL1 fluxes, and tested by Static Extraction Method, contamination shall<sup>2</sup> be less than 1.56 micrograms/cm<sup>2</sup> sodium chloride (NaCl) equivalent ionic or ionizable flux residue. When another test method or flux is used (see 3.3), contamination shall **not**<sup>2</sup> exceed a limit to be established by the manufacturer or by the user. When established by the manufacturer, the limit shall<sup>2</sup> be supported by historical data (indicating that

the cleaning and testing processes are proven, well established, and in control), or by process qualification test data (see 3.1) that are available for review.

(2) Class 1-Defect Class 2-Defect Class 3-Defect

8.3.6.3 Ionic Residues (Manual Method) When ionic residue (manual method) testing is required, assemblies shall<sup>3</sup> be tested in accordance with IPC-TM-650, Test Method 2.3.25, Detection and Measurement of Ionizable Surface Contaminants.

For assemblies soldered with ROL0 or ROL1 fluxes, surface contamination shall<sup>3</sup> be less than 1.56 micrograms/ cm<sup>2</sup> NaCl equivalent ionic or ionizable flux residue. When another flux is used (see 3.3), contamination shall not<sup>3</sup> exceed a limit to be established by the manufacturer or by

the user. When established by the manufacturer, the limit shall<sup>3</sup> be supported by historical data (indicating that the cleaning process is proven,

(3) Class 1-Defect Class 2-Defect Class 3-Defect well established, and in control), or by process qualification test data (see 3.1) that are available for review.

## 8.3.6.4 Surface Insulation Resistance (SIR) When sur-

face insulation resistance testing (SIR) is required, it shall<sup>4</sup> be performed using a documented method that includes pass/fail criteria and is available for review.

(4) Class 1-Defect Class 2-Defect Class 3-Defect

8.3.6.5 Other Contamination When surface organic contamination testing is required, assemblies tested in accordance with IPC-TM-650, Test Method 2.3.39, Surface Organic Contamination Identification Test (Infrared Ana-

lytical Method) shall not<sup>5</sup> exceed the maximum acceptance level established by mutual agreement between user and manufacturer.

(5) Class 1-Defect Class 2-Defect Class 3-Defect

### 9 PCB REQUIREMENTS

This section applies to PCB defects regardless of when they occur.

### 9.1 Printed Circuit Board Damage

9.1.1 Blistering/Delamination Blistering or delamina-

tion(s) shall not<sup>6</sup> exceed 25% of the distance between plated-through holes or internal conductors or reduce the space between conductive patterns below the minimum electrical clearance.

(6) Class 1-Defect Class 2-Defect Class 3-Defect

**Note:** Blisters or delamination areas may propagate during assembly or operation. Separate criteria may need to be established. Measling is NOT the same as blistering and/or delamination. See IPC-T-50 and IPC-A-610 for clarification.

9.1.2 Weave Exposure Weave exposure shall not<sup>7</sup> reduce the clearance between noncommon conductive patterns to less than the minimum electrical clearance.

(7) Class 1-Defect Class 2-Defect Class 3-Defect

9.1.3 Haloing Penetration of haloing or edge delamination shall not<sup>8</sup> affect the physical spacing from the edge to the closest conductive pattern by more than 50% or more than 2.5 mm [0.0984 in], whichever is less.

(8) Class 1-Defect Class 2-Defect Class 3-Defect

9.1.4 Land Separation The outer, lower edge of land areas shall not<sup>9</sup> be lifted or separated more than the thickness (height) of the land.

9.1.5 Land/Conductor Reduction in Size The minimum

width of printed conductors or width/ length of lands shall not<sup>1</sup> be reduced by more than 20% for Class 2 and 3 and 30% for Class 1 (see IPC-A-600, IPC-6011 and IPC-6012).

(1) Class 1-Defect Class 2-Defect Class 3-Defect

9.1.6 Flexible Circuitry Delamination Separation or bubbles shall not<sup>2</sup> bridge conductors in the cover layer of flexible printed circuit boards or assemblies.

(2) Class 1-Defect Class 2-Defect Class 3-Defect

9.1.7 Flexible Circuitry Damage There shall not<sup>3</sup> be

evidence of blistering, charring, or melting of the insulation on flexible printed circuit boards or assemblies.

(3) Class 1-Defect Class 2-Defect Class 3-Defect

Note: Mechanically created indentions caused by contact between the coverlayer of flexible printed circuit boards or assemblies and molten solder are not rejectable. Additionally, care should be taken to avoid bending or flexing conductors during inspection.

**9.1.8 Burns** Burns shall not<sup>4</sup> physically damage the surface of the assembly.

(4) Class 1-Defect Class 2-Defect Class 3-Defect

9.1.9 Solder on Gold Contacts Solder shall not<sup>5</sup> be in the contact area of gold edge connector contact lands (i.e., "gold fingers").

(5) Class 1-Defect Class 2-Defect Class 3-Defect

9.1.10 Measles Measled areas in laminate substrates shall not<sup>6</sup> exceed 50% of the physical spacing between internal conductors.

(6) Class 1-Not Est Class 2-Proc Ind Class 3-Defect

Note: Visual aids can be found in IPC-A-610 and IPC-HDBK-001.

9.2 Marking Assembly identification such as part numbers and serial numbers shall<sup>7</sup> remain legible (capable of being read and understood) after all tests, cleaning and other processes to which the item is subjected. Additional markings (such as labels added during the manufacturing process) should not obscure the original supplier's mark-

ings. Individual component markings, reference designators and polarity indicators should remain legible and components should be mounted in

(7) Class 1-Not Est Class 2-Defect Class 3-Defect

such a manner that markings are visible.

9.3 Bow and Twist (Warpage) Bow and twist after soldering should not exceed 1.5% for through-hole, or 0.75% for surface mount printed board applications (see IPC-TM- 650, 2.4.22). Bow and twist **shall not**<sup>8</sup> cause damage during post solder assembly operations or use.

(8) Class 1-Defect Class 2-Defect Class 3-Defect

### 10 COATING AND ENCAPSULATION

When coating or encapsulation materials are applied to glass body components, the components shall<sup>9</sup> be sleeved to prevent cracking, unless the material has been selected so as not to damage the

(9) Class 1-Defect Class 2-Defect Class 3-Defect

components/assembly in its service environment.

## 10.1 Conformal Coating

Conformal coating material shall<sup>10</sup> conform to the material specification (IPC-CC-830 or equivalent). The coating manufacturers supplier's instructions or other documented process shall<sup>10</sup> be followed.

When curing conditions (temperature, time, Infra Red (I.R.) intensity, etc.) vary from supplier recommended instructions, they shall 10 be documented and available for review.

The material shall<sup>10</sup> be used within the time period specified (both shelf life and pot life) or used within the time period indicated by a documented system the manufacturer (assembler) has established to mark and control age-dated material.

(10) Class 1-Defect Class 2-Defect Class 3-Defect

10.1.1 Application Coating shall<sup>11</sup> be applied in a continuous manner to all areas designated for coverage on the assembly drawing/documentation.

The coating fillets should be kept to a minimum. When used, masking materials shall<sup>11</sup> have no deleterious effect and shall<sup>11</sup> be removable without leaving contaminant resi-

Dimensions of masked areas shall not<sup>11</sup> be decreased in length, width, or diameter by more than 0.75 mm [0.0295 in] by application of conformal coating.

(11) Class 1-Defect Class 2-Defect Class 3-Defect

10.1.1.1 Components Required to be Uncoated The adjustable portion of adjustable components, as well as electrical and mechanical mating surfaces such as connec-

tor contacts, probe points, screw threads, bearing surfaces (e.g., card guides) shall<sup>12</sup> be left uncoated as specified on the assembly drawing(s)/ documentation.

(12) Class 1-Defect Class 2-Defect Class 3-Defect

10.1.1.2 Conformal Coating on Connectors Mating connector surfaces of printed circuit assemblies shall **not**<sup>13</sup> be coated with conformal coating.

The conformal coating specified on the assembly drawing(s)/ documentation should, however, provide a seal around the perimeter of all connector/board interface areas.

### 10.1.1.3 Conformal Coating on Brackets The mating

(contact) surface of brackets or other mounting devices **shall not**<sup>1</sup> be coated with conformal coating unless specifically required by the assembly drawing(s)/documentation.

(1) Class 1-Defect Class 2-Defect Class 3-Defect

### 10.1.2 Performance Requirements

**10.1.2.1 Thickness** The thickness of the conformal coating **shall**<sup>2</sup> be as shown in Table 10-1 for the type specified (see IPC-2221):

(2) Class 1-Defect Class 2-Defect Class 3-Defect

**Note:** Table 10-1 of this standard is to be used for printed circuit assemblies. The coating thickness requirements in IPC-CC-830 Table 4-2 are to be used only for test vehicles associated with coating material testing and qualification.

Table 10-1 Coating Thickness

		•
Type AR	Acrylic Resin	0.03-0.13 mm [0.00118 to 0.00512 in]
Type ER	Epoxy Resin	0.03-0.13 mm [0.00118 to 0.00512 in]
Type UR	Urethane Resin	0.03-0.13 mm [0.00118 to 0.00512 in]
Type SR	Silicone Resin	0.05-0.21 mm [0.00197 to 0.00827 in]
Type XY	Paraxylylene Resin	0.01-0.05 mm [0.000394 to 0.00197 in]

The thickness is measured on a flat, unencumbered, cured surface of the printed circuit assembly or a coupon that has been processed with the assembly. Coupons may be of the same type of material as the printed board or may be of a nonporous material such as metal or glass. As an alternative, wet film or viscosity measurement may be used to establish the coating thickness provided there is documentation that correlates dry film thickness to the alternate measurement technique.

## **10.1.2.2 Coating Coverage** Conformal coating **shall**<sup>3</sup>:

Be completely cured and homogeneous.

(3) Class 1-Defect Class 2-Defect Class 3-Defect

- Cover only those areas specified on the assembly drawing(s)/documentation.
- Be free of blisters, or breaks that could affect the operations of the assembly or sealing properties of the conformal coating.
- Be free of cracks, crazing, voids, bubbles, mealing, peeling, wrinkles or foreign material which expose component conductors, printed circuit conductors, (including

ground planes) or other conductors and/or violates design electrical clearance.

**10.1.3 Conformal Coating Inspection** Visual inspection of conformal coating may be performed without magnification. Inspection for conformal coating coverage may be performed under an ultraviolet (UV) light source when using conformal coating material containing a UV tracer. Magnification up to 4X may be used for referee purposes.

**10.2 Encapsulation** The material specification and supplier's instructions, as applicable, **shall**<sup>4</sup> be followed. The material **shall**<sup>4</sup> be used within the time period specified

(both shelf life and pot life) or used within the time period indicated by a documented system the manufacturer has established to mark and control age-dated material.

(4) Class 1-Defect Class 2-Defect Class 3-Defect

**10.2.1 Application** Encapsulant material **shall**<sup>5</sup> be applied in a continuous manner to all areas designated for

coverage on the assembly drawing/documentation. When used, masking material **shall**<sup>5</sup> have no deleterious effect on the printed boards and **shall**<sup>5</sup>

(5) Class 1-Defect Class 2-Defect Class 3-Defect

be removable without contaminant residue.

**10.2.1.1 Encapsulant Free Surfaces** All portions of the assembly not designated to receive encapsulant material **shall**<sup>6</sup> be free of any encapsulant material.

(6) Class 1-Defect Class 2-Defect Class 3-Defect

**10.2.2 Performance Requirements** The applied encapsulant **shall**<sup>7</sup> be completely cured, homogeneous, and cover

only those areas specified on the assembly drawing(s)/documentation. The encapsulant **shall**<sup>8</sup> be free of bubbles, blisters, or breaks that affect the printed circuit assembly operation or sealing properties of the encapsulant material. There **shall**<sup>9</sup> be no visible cracks, crazing, mealing, peeling, and/or wrinkles in the encapsulant material.

(7) Class 1-Not Est Class 2-Defect Class 3-Defect (8) Class 1-Defect

Class 2-Defect Class 3-Defect

(9) Class 1-Not Est Class 2-Proc Ind Class 3-Defect

10.2.3 Rework of Encapsulant Material Procedures which describe the removal and replacement of encapsulant material shall<sup>10</sup> be documented and available for review.

(10) Class 1-Not Est Class 2-Not Est Class 3-Defect

**10.2.4 Encapsulant Inspection**Visual inspection of encapsulation

shall<sup>11</sup> be performed per 11.2.

(11) Class 1-Accept Class 2-Proc Ind Class 3-Defect

#### 11 PRODUCT ASSURANCE

11.1 Hardware Defects Requiring Disposition Hardware defects that require disposition are annotated throughout the standard and are summarized in Appendix A. A defect shall not<sup>1</sup> be reworked before

defect **shall not**<sup>1</sup> be reworked before it is documented per 12.1. Touch-up processes that include reheating are examples of rework operations.

(1) Class 1-Not Est Class 2-Not Est Class 3-Defect

### 11.2 Inspection Methodology

**11.2.1 Process Verification Inspection** Process verification inspection **shall**<sup>2</sup> consist of the following:

(2) Class 1-Not Est
Class 2-Not Est
Class 3-Defect

- a. Surveillance of the operation to determine that practices, methods, procedures and a written inspection plan are being properly applied.
- b. Inspection to measure the quality of the product.
- **11.2.2 Visual Inspection** The assembly **shall**<sup>3</sup> be evaluated in accordance with the established process control plan (see 11.3) or by 100% visual inspection (see 1.11).

(3) Class 1-Not Est Class 2-Defect Class 3-Defect

**11.2.2.1 Magnification Aids** Magnification power for visual inspection **shall**<sup>4</sup> be at least the minimum inspection power specified in Tables 11-1

(4) Class 1-Accept Class 2-Proc Ind Class 3-Defect

and 11-2. Other magnification powers within the inspection range may be used. The magnification power requirement is based on the size of the device being inspected. For assemblies with mixed land widths, the greater magnification may be used for the entire assembly. If the presence of a defect cannot be determined at the inspection power, the item is acceptable. The referee magnification power is intended for use only after a defect has been determined but is not completely identifiable at the inspection power.

The tolerance for magnification aids is  $\pm$  15% of the selected magnification power. Magnification aids should be maintained and calibrated as appropriate (see IPC-OI-645). Supplemental lighting may be necessary to assist in visual assessment.

- **11.2.2.2 Lighting** Supplemental lighting may be necessary to assist in visual inspection. Light sources should be selected to prevent shadows on the item being inspected except those caused by the item being inspected.
- **11.2.3 Sampling Inspection** Use of sample-based inspection **shall**<sup>5</sup> be done only as part of a documented process control system per 11.3.

(5) Class 1-Not Est Class 2-Proc Ind Class 3-Defect

Table 11-1 Magnification Aid Applications for Solder Connections

	Magnification Power		
Land Widths or Land Diameters <sup>1</sup>	Inspection Range	Maximum Referee	
> 1.0 mm [0.0394 in]	1.5X to 3X	4X	
>0.5 to ≤1.0 mm [0.0197 to 0.0394 in]	3X to 7.5X	10X	
≥0.25 to ≤0.5 mm [0.00984 to 0.0197 in]	7.5X to 10X	20X	
<0.25 mm [0.00984 in]	20X	40X	

Note 1. A portion of a conductive pattern used for the connection and/or attachment of components.

Table 11-2 Magnification Aid Applications - Other

Cleanliness (cleaning processes per 8.3.4)	Magnification not required, see Note 1
Cleanliness (no-clean processes per 8.3.4)	Note 1
Conformal Coating/ Encapsulation (10.1.4 and 10.2.4)	Notes 1,2
Other (Component and wire damage, etc.)	Note 1

Note 1. Visual inspection may require the use of magnification, e.g. when fine pitch or high density assemblies are present, magnification may be needed to determine if contamination affects form, fit or function.

Note 2. If magnification is used it is limited to 4X maximum.

**11.3 Process Control Requirements** The primary goal of process control is to continually reduce variation in the processes, products, or services to provide products or processes meeting or exceeding customer requirements. Process control tools such as IPC-9191, EIA-557-1 or other user-approved system may be used as guidelines for implementing process control.

Manufacturers of Class 3 products **shall**<sup>6</sup> develop and implement a documented process control system.

A documented process control system, if established, **shall**<sup>7</sup> define process control and corrective action limits. This may or may not be a "statistical process control" system. The use of "statistical process control" (SPC) is optional and should be based on factors such as design stability, lot size, production quantities, and the needs of the manufacturer (see 11.4).

Process control methodologies **shall**<sup>7</sup> be used in the planning, implementation and evaluation of the manufacturing processes used to produce soldered electrical and electronic

assemblies. The philosophy, implementation strategies, tools and techniques may be applied in different sequences depending on the specific company, operation, or variable under consideration to relate process control and capability to end product requirements.

(6) Class 1-Not Est Class 2-Not Est Class 3-Defect(7) Class 1-Not Est Class 2-Defect

Class 3-Defect

When a decision or requirement is to use a documented process control system, failure to implement process cor-

rective action and/or the use of continually ineffective corrective actions **shall**<sup>1</sup> be grounds for disapproval of the process and associated documentation.

(1) Class 1-Not Est Class 2-Defect Class 3-Defect

11.3.1 Opportunities Determination Unless otherwise specified in the process control plan, the total number of interconnection sites is used as the measure to which the percentage of defects or process indicators is applied. These calculations consider each surface mount termination, each through-hole termination, and each terminal termination as a single opportunity in determining the total number of opportunities for a given printed board assembly. For corrective action calculations, no more than one defect characteristic or process indicator can be attributed to a particular interconnection site (e.g., via, lead-in-hole, lead-to-land). For more information (see IPC-9261).

**11.4 Statistical Process Control** The use of "statistical process control" is encouraged but not mandatory (see 11.3).

When a statistical process control system process is used, it **shall**<sup>2</sup> include the following elements as a minimum:

(2) Class 1-Defect Class 2-Defect Class 3-Defect

- a. Training is provided to personnel with assigned responsibilities in the development, implementation, and utilization of process control and statistical methods that are commensurate with their responsibilities.
- b. Quantitative methodologies and evidence is maintained to demonstrate that the process is capable and in control. Improvement strategies define initial process control limits and methodologies leading to a reduction in the occurrence of process indicators in order to achieve continuous process improvement.
- c. Criteria for switching to sample based inspection is defined. When processes exceed control limits, or demonstrate an adverse trend or run, the criteria for reversion to higher levels of inspection (up to 100%) is also defined.

- d. When defect(s) are identified in the lot sample, and the number exceeds the limit allowed by the sampling plan, the entire lot is 100% inspected for the occurrence(s) of the defect(s).
- e. A system is in place to initiate corrective action for the occurrence of process indicators, out-of-control process(es), and/or discrepant assemblies.
- A documented audit plan is defined to monitor process characteristics and/or output at a prescribed frequency.
- g. Objective evidence of process control may be in the form of control charts or other tools and techniques of statistical process control derived from application of process parameter and/or product parameter data (see IPC-HDBK-001).

### 12 REWORK AND REPAIR

**12.1 Rework of Unsatisfactory Solder Connections** Rework for Classes 1 or 2 should be documented. The following requirements **shall**<sup>3</sup> be followed for Class 3:

(3) Class 1-Not Est Class 2-Not Est Class 3-Defect

- A hardware defect is documented before rework.
- When rework is performed, each reworked and/or reflowed connection is inspected to the requirements of 4.14.
- **12.2 Repair** A hardware defect **shall not**<sup>4</sup> be repaired until the discrepancy has been documented. The repair method **shall**<sup>4</sup> be determined by

(4) Class 1-Not Est Class 2-Defect Class 3-Defect

agreement between the manufacturer and the user.

**12.3** Post Rework/Repair Cleaning After rework or repair assemblies **shall**<sup>5</sup> be cleaned as necessary by a process meeting the requirements of 8.3.

(5) Class 1-Not Est Class 2-Not Est Class 3-Defect

**12.4 Rework of Conformal Coating/ Encapsulant** Procedures which describe the rework of conformal coating/encapsulant **shall**<sup>6</sup> be documented and available for review.

(6) Class 1-Not Est Class 2-Not Est Class 3-Defect

Appendix A Summary of Criteria Requiring Disposition to Nonconforming Conditions

"A" = Acceptable "P" = Process Indicator "D" = Defect, "N" = No Requirement Established		Reference		Class 1	Class 2	Class 3
Nonconforming materials or processes.	1.5.1 1.5.2 1.9 1.11 1.12 1.13.2.1 3.1 3.2 3.3 3.3.1 3.4 3.5 3.6 3.7 3.8 3.9 3.91	3.9.2 3.9.4 3.11 4.1 4.2 4.3 4.9 4.9.1 4.9.4 4.10 4.11.2 5.1 5.1.1 5.3.3 6.1 7.1 7.1.3	7.1.6 8.3.2 8.3.6 8.3.6.1 8.3.6.2 8.3.6.3 8.3.6.4 8.3.6.5 9.3 10.1 10.1.1 10.2 10.2.1 11.4	D	D	D
	1.10 1.13 3.2.2 3.9.7 4.2.2 4.9.2 4.11.1	4.11.2 4.12 5.1.1 5.3.4 5.3.5 6.1.4 6.3.1	8 9.2 10.2.2 11.2.2 11.3 12.2	N	D	D
	1.13 3.1 3.3 4.2.4 4.11.2.1 4.12 6.1.4	7.1.4 7.3 7.4 7.5 8 10.2.3 11.1	11.2.1 11.3 12.1 12.3 12.4	N	N	D
Terminals modified to accept oversize conductors.			5.2	N	D	D
Gold not removed as required.			3.9.3	N	Р	D
Components, leads and wires.	3.9.5 3.9.6	6.1.1 6.1.2	7.1.1 7.1.3	D	D	D
		6.1.1	7.1.3	Α	Р	D
Insulation and wire damage.	1.13.2.3	5.1	5.4.1.6	D	D	D
			5.1	Α	D	D
Mounted parts and components.			4.4	Α	Р	D
Adhesives.			4.6	D	D	D
		504	4.6	A	P	D
Terminal has damage.  Violation of minimum electrical clearance.		5.3.1	5.3.2	D	D	D
Insulation in solder.			1.8.4	D A	D D	D D
			5.4.1			_
Service loops that do not conform to the requirements.  No stress relief.		5.4.1.3	5.4.1.2 5.4.1.5	N D	P D	D D
NO Stress relief.		3.4.1.3	5.4.1.3	A	P	D
Sleeving fits incorrectly.			5.4.1.6	A	D	D
Orientation, dress, fill or termination of wire/lead does not conf	form to require	ments	5.4.5	A	D	D
Shortagen, group, in or termination of whoreas does not com	om to require		5.4.6	N	P	D
	5.4.1.1 5.4.1.4 5.4.1.5 5.4.2.1	5.4.2.2 5.4.2.3 5.4.2.4	5.4.3 5.4.4 5.4.6	A	P	D

"A" = Acceptable "P" = Process Indicator "D" = Defect, "N" = No Requirement Established		Reference		Class 1	Class 2	Class 3
Lead clinches.			6.1.3	D	D	D
			6.1.3	N	D	D
Lead protrusion.			6.1.3	D	D	D
Failure to comply with the cleanliness requirements.  4.8				D	D	D
Violation of the assembly drawing requirements.		'	1.11	D	D	D
Damage to printed wiring assembly in excess of that allowed.	9.1 9.2 9.3	9.4 9.5 9.6	9.7 9.8 9.9	D	D	D
			9.1.10	N	Р	D
Solder connections that do not conform to the requirements.		4.14	4.14.3	D	D	D
Terminal connections.	4.14 4.14.3 5.3.6	5.4.1.1 5.4.3 5.5	5.5.1 5.5.2	D	D	D
			5.5.2	N	Р	D
Through-hole connections.	4.13 4.14 4.14.3	6.1.3 6.1.6 6.2.1	6.3.2	D	D	D
Surface mount connections.	4.14 4.14.3 7.6 7.6.3 7.6.4 7.6.5	7.6.6 7.6.7 7.6.8 7.6.9 7.6.10 7.6.11	7.6.12 7.6.13 7.6.14 7.6.15 7.6.16	D	D	D
Conformal coating and encapsulation.	10.1.1.1 10.1.1.2 10.1.1.3	10.1.2.1 10.1.2.2 10.2.1.1	10.2.2	D	D	D
			10.2.2	N	Р	D
Wires used at a potential of 6kV or greater do not meet requirements.			1.13.2.3	D	D	D
Inspection methods.			11.2.3	N	Р	D
			11.2.2.1	Α	Р	D

# Appendix B Guidelines for Soldering Tools and Equipment

The following guidelines for tools and equipment selection and use have been found through industry practice to be effective in meeting the requirements of this standard (see 1.7.3).

#### **B-1 ABRASIVES**

Knives, emery cloth, sandpaper, sandblasting, braid, steel wool, and other abrasives are not to be used on surfaces to be soldered.

### **B-2 BENCHTOP AND HAND SOLDERING SYSTEMS**

Selection criteria of benchtop and hand soldering systems include:

- a. Soldering systems are selected for their capacity to heat the connection area rapidly and maintain sufficient soldering temperature range at the connection throughout the soldering operation.
- b. Temperature controlled soldering equipment (at rest) should be controlled within  $\pm$  5°C [ $\pm$  9°F] of the idle tip temperature. Constant output (steady output) tools in compliance with B-2a, d, e, & f may also be used.
- c. Operator selected or rated temperatures of soldering systems at idle/standby should be within  $\pm\,15^{\circ}\text{C}$  [ $\pm\,27^{\circ}\text{F}$ ] of actual measured tip temperature.
- d. Resistance between the tip of soldering systems and the workstation common point ground should not exceed 5 ohms. Heated element and tips are measured when at their normal operating temperature.

**Note:** Current limiting soldering equipment manufactured to EN 00015-1:1992 may not meet this requirement.

- e. AC and DC current leakage from heated tip to ground should not create deleterious effects on equipment/ components.
- f. Tip transient voltages generated by the soldering equipment should not exceed 2V peak  $(Z_{in} \ge \Omega)$ .

**Note:** Current limiting soldering equipment manufactured to EN 00015-1:1992 may not meet this requirement.

The appropriate guidelines of this section also apply to nonconventional benchtop soldering equipment; including equipment which utilizes conductive, convective, parallel gap resistance, shorted bar resistance, hot gas, infrared, laser powered devices, or thermal transfer soldering techniques. Tools used are to be maintained such that no detrimental damage results from their use. Tools and equipment are to be clean prior to use and should be kept clean and free of dirt, grease, flux, oil and other foreign matter dur-

ing use. The heat source is not to cause damage to the printed board or components.

### **B-3 HEATED SOLDERING TOOL HOLDERS**

Soldering tool holders are to be of a type appropriate for the soldering tool used. The holder should leave the soldering tool heating element and tip unsupported without applying excessive physical stress or heat sinking and is to protect personnel from burns.

#### **B-4 WIPING PADS**

Sponges and pads for wipe cleaning of soldering iron tips and reflow soldering tool surfaces are to be manufactured from materials which are not detrimental to solderability or which could contaminate soldering tool surfaces. The operator is to keep sponges and pads free of contaminants that are detrimental to solderability or that would contaminate the soldering tool surfaces.

### **B-5 SOLDERING GUNS**

Soldering guns with the transformer incorporated into the hand piece are not to be used.

### **B-6 SOLDER POTS**

Solder pots should maintain the solder temperature within  $\pm 5^{\circ}\text{C}$  [ $\pm 9^{\circ}\text{F}$ ] of the selected temperature. Solder pots are to be grounded.

### **B-7 USE AND CONTROL**

All equipment is to be operated in accordance with manufacturers' recommendations and calibrated where necessary to maintain manufacturers' specifications. Equipment grounding, protection and temperature control testing should be performed when qualifying equipment for purchase and/or inspection of new or repaired equipment.

## **B-8 MACHINE SOLDERING SYSTEMS**

The design of automated machine soldering systems should provide:

- a. The capability to preheat printed wiring assemblies.
- b. The capacity to maintain the soldering temperature at the assembly surface within  $\pm 5^{\circ}\text{C}$  [ $\pm 9^{\circ}\text{F}$ ] of the selected temperature throughout the span of any continuous soldering run.
- c. The capability to rapidly heat the surfaces to be joined and the capacity to reattain the present temperature within  $\pm$  5°C [ $\pm$  9°F] during repetitive soldering operations.

The heat source is not to cause damage to the printed board or components, or contaminate the solder when direct contact is made between the heat source and metals to be joined.

Soldering equipment should be utilized in accordance with a documented process that is available for user review.

**B-8.1 Carriers** Devices used for the transport of printed boards through preheat, soldering, and cooling stages should be of such material, design, and configuration that

they will not cause board, part or component degradation or ESD damage to components.

### **B-9 MACHINE MAINTENANCE**

Machines related to the soldering process are to be maintained to assure capability and efficiency commensurate with design parameters established by the original equipment manufacturer. Maintenance procedures and schedules should be documented in order to provide reproducible processing.

# Appendix C Material and Process Compatibility Testing

#### C-1 SCOPE/INTRODUCTION

- **C-1.1 Scope** This appendix sets forth a standardized testing protocol to be used when:
- Implementing flux materials other than those noted in 3.3.
- Validating the acceptability of a major change in a proven process prior to its implementation in an electronics manufacturing process.

The testing protocol covers printed wiring assemblies using surface mount technology (SMT), plated-through hole (PTH) or mixed technology (both SMT and PTH).

**C-1.2 Intent** The intent of the testing, outlined in this protocol, is to show that a proposed manufacturing process change can produce hardware with acceptable end-item performance.

These process changes can involve a change in one of the process steps. They can also pertain to a change in bare board supplier, solder resist or metallization. Test vehicle construction will vary depending upon which of these changes is being evaluated.

**Note:** This testing is a "site specific" qualification process to be done at the manufacturer's location using production processes and equipment whenever possible.

### C-2 TEST APPROACH

## C-2.1 Surface Insulation and Visual Inspection

- **C-2.1.1 Surface Insulation Resistance (SIR)** SIR testing is an evaluation of the effects of the material/process on electrical performance.
- **C-2.1.2 Visual Inspection** Visual inspection of samples after SIR notes presence of corrosion, dendritic formation or mealing of conformal coating.
- **C-2.2 Extractive Tests OPTIONAL** Recommended test techniques that can be used to characterize residues for process control purposes are as follows:
- C-2.2.1 Resistivity of Solvent Extract (ROSE) ROSE testing in accordance with IPC-TM-650, Method 2.3.25, Detection and Measurement of Ionizable Surface Contaminants, can be used to establish a baseline for ionic contamination after the complete assembly process, which may or may not include cleaning depending upon what flux is used.

**C-2.2.2 Ion Chromatography (IC)** IC testing in accordance with IPC-TM-650, Method 2.3.28, is especially helpful for identification/quantification of ionic species during initial process characterization or during failure analysis of test assemblies.

### **C-3 TEST ASSEMBLY**

The test vehicle should represent the substrate materials, assembly materials and fabrication processes used in the production. The test vehicle circuitry must provide for SIR testing similar to the IPC-B-36 circuitry. Components of the type to be soldered in production representative of the "'hardest-to-clean" configurations (in terms of "shadowing" of the solder connections by component bodies and component-to-substrate spacing) need to be included on the PWA.

Test patterns used for SIR testing must be free of permanent solder resist.

Boards used in these test assemblies must meet the requirements of IPC-6011 and IPC-6012 appropriate product class.

**Note:** Contact IPC for information on commercially available SIR test vehicles.

### C-4 TEST ASSEMBLY PREPARATION

- **C-4.1 Precleaning** No cleaning prior to assembly is to be done on the PCBs used in these tests that is not done as part of the standard assembly process.
- C-4.2 Processing of Test Assemblies The manufacturing process used in this protocol is assumed to be as close as possible to the process intended for production hardware. In cases where the assembly process involves multiple solder operations (e.g., surface mount reflow, wave solder, rework, hand solder, or conformal coating if used), all these processes must be done on the test assembly. This would be necessary even in cases where only one of the soldering processes is being changed, since residues from one process can interact with residues from a prior or following process. It is the total of all these processes that will be shipped and thus it is their total that must be tested and qualified.

### C-5 SIR TESTING

See IPC-9201 for a discussion of the proper methodology and equipment to be used for repeatable and accurate SIR testing.

**C-5.1 Sample Size** A minimum of 10 vehicles need to be tested for each material/process combination. This sample size was calculated by setting a "consumers risk" at 10 (confidence of 90). A complete explanation of how this sample size was determined can be found in IPC-TR-467. It is recommended that additional unprocessed vehicles be tested as controls.

### C-5.2 SIR Test Conditions

**C-5.2.1 Noncondensing Service Environment** Test vehicles need to be tested in accordance with IPC-TM-650, Method 2.6.3.3.

C-5.2.2 Condensing Service Environment All test vehicles need to be exposed to the conditions noted in IPC-TM-650, Method 2.6.3, Class 3. Measurements need to be taken at the upper temperature and humidity level of every third cycle (starting with the third cycle).

**Note:** This is a condensing environment. Test assemblies exposed to this environment need to be conformally coated using the same coating material/application processes used in "delivered" hardware.

### C-6 ACCEPTANCE CRITERIA

**C-6.1 Convert the minimum SIR value from each test vehicle to log10** The average of these log values less 3 standard deviations (of log values) needs to be at least 8.0 (1E8 Ohm).

**Note:** The minimum values used should be from one specific test pattern design. If multiple test pattern designs are used on a test vehicle, each set of data must meet the requirements.

**C-6.2 Visual Requirements** All biased sites need to have the components removed without application of chemicals or heat, preferably by cutting of leads. All areas need to be inspected at 10X - 30X for corrosion and dendritic formation. Backlighting should be used to inspect for dendritic formation.

There is to be no evidence of corrosion. Dendritic formation cannot bridge more than 20% of the distance between conductors. Conformally coated PCAs need to exhibit evidence of reversion, cracking or mealing.

### C-7 REPORTING

The test report needs to include the following information:

- Substrate information: laminate type, solder resist, final finish (SMOBC/HASL, reflow, OSP, etc.), and final cleaning.
- Assembly information: manufacturing process, equipment, and materials.
- · Conformal coating if used.
- Test vehicle description (e.g., P/N, type of assembly, components used).
- SIR test environment and results.
- Results of post SIR test visual inspection.

## Appendix D

## Minimum Electrical Clearance - Electrical Conductor Spacing

NOTE: Appendix D is quoted from IPC-2221 Generic Standard on Printed Board Design (February 1998) and is provided for information only. It is current as of publication date of this document. The user has the responsibility to determine the most current revision level of IPC-2221 and specify the specific application to their product. Paragraph and table numbers are from IPC-2221.

The following statement from IPC-2221 applies to this Appendix ONLY: **1.4 Interpretation** – "Shall," the imperative form of the verb, is used throughout this standard [IPC-A-610C Appendix A] whenever a requirement is intended to express a provision that is mandatory.

*IPC-2221* – **6.3 Electrical Clearance** Spacing between conductors on individual layers should be maximized whenever possible. The minimum spacing between conductors, between conductive patterns, layer to layer conductive spaces (z=axis), and between conductive materials (such as conductive markings or mounting hardware) and conductors **shall** be in accordance with Table 6-1, and defined on the master drawing. See Section 10 for additional information on process allowances affecting electrical clearance.

When mixed voltages appear on the same board and they require separate electrical testing, the specific areas **shall** be identified on the master drawing or appropriate test specification. When employing high voltages and especially AC and pulsed voltages greater than 200 volts potential, the dielectric constant and capacitive division effect of the material must be considered in conjunction with the recommended spacing.

For voltages greater than 500V, the (per volt) table values must be added to the 500V values. For example, the electrical spacing for a Type B1 board with 600V is calculated as:

600V - 500V = 100V 0.25 mm [0.00984 in] + (100V x 0.0025 mm) = 0.50 mm [0.0197 in] clearance

When, due to the criticality of the design, the use of other conductor spacings is being considered, the conductor spacing on individual layers (same plane) **shall** be made larger than the minimum spacing required by Table 6-1 whenever possible. Board layout should be planned to allow for the maximum spacing between external layer conductive areas associated with high impedance or high voltage circuits. This will minimize electrical leakage problems resulting from condensed moisture or high humidity. Complete reliance on coatings to maintain high surface resistance between conductors **shall** be avoided.

*IPC-2221* **-6.3.1 B1-Internal Conductors** Internal conductor-to-conductor, and conductor-to-plated-through hole electrical clearance requirements at any elevation (see Table 6-1).

*IPC-2221* – **6.3.2 B2-External Conductors, Uncoated, Sea Level to 3050 m [10,007 feet]** Electrical clearance requirements for uncoated external conductors are significantly greater than for conductors that will be protected from external contaminants with conformal coating. If the assembled end product is not intended to be conformally coated, the bare board conductor spacing **shall** require the spacing specified in this category for applications from sea level to an elevation of 3050 m [10,007 feet] (see Table 6-1).

*IPC-2221* – **6.3.3 B3-External Conductors, Uncoated, Over 3050 m [10,007 feet]** External conductors on uncoated bare board applications over 3050 m [10,007 feet] require even greater electrical spacings than those identified in category B2 (see Table 6-1).

*IPC-2221* – **6.3.4 B4-External Conductors**, **with Permanent Polymer Coating (Any Elevation)** When the final assembled board will not be conformally coated, a permanent polymer coating over the conductors on the bare board will allow for conductor spacings less than that of the uncoated boards defined by category B2 and B3. The assembly electrical clearances of lands and leads that are not conformally coated require the electrical clearance requirements stated in category A6 (see Table 6-1). This configuration is not applicable for any application requiring protection from harsh, humid, contaminated environments.

Typical applications are computers, office equipment, and communication equipment, bare boards operating in controlled environments in which the bare boards have a permanent polymer coating on both sides. After they are assembled and soldered the boards are not conformal coated, leaving the solder joint and soldered land uncoated.

**Note:** All conductors, except for soldering lands, must be completely coated in order to ensure the electrical clearance requirements in this category for coated conductors.

*IPC-2221* – **6.3.5 A5-External Conductors, with Conformal Coating Over Assembly (Any Elevation)** External conductors that are intended to be conformal coated in the final assembled configuration, for applications at any elevation, will require the electrical clearances specified in this category.

Typical applications are military products where the entire final assembly will be conformal coated. Permanent

polymer coatings are not normally used, except for possible use as a solder resist. However, the compatibility of polymer coating and conformal coating must be considered, if used in combination.

*IPC-2221* – 6.3.6 A6-External Component Lead/ Termination, Uncoated, Sea Level to 3050 m [10,007 feet] External component leads and terminations, that are not conformal coated, require electrical clearances stated in this category.

Typical applications are as previously stated in category B4. The B4/A6 combination is most commonly used in

commercial, nonharsh environment applications in order to obtain the benefit of high conductor density protected with permanent polymer coating (also solder resist), or where the accessibility to components for rework and repair is not required.

IPC-2221 - 6.3.7 A7-External Component Lead/ Termination, with Conformal Coating (Any Elevation) As in exposed conductors versus coated conductors on bare board, the electrical clearances used on coated component leads and terminations are less than for uncoated leads and

IPC-2221 - Table 6-1 Electrical Conductor Spacing

terminations.

Voltage Between	Minimum Spacing							
Conductors	Bare Board				Assembly			
(DC or AC Peaks)	B1	B2	В3	B4	A5	A6	A7	
0-15	0.05 mm	0.1 mm	0.1 mm	0.05 mm	0.13 mm	0.13 mm	0.13 mm	
	[0.00197 in]	[0.0039 in]	[0.0039 in]	[0.00197 in]	[0.00512 in]	[0.00512 in]	[0.00512 in]	
16-30	0.05 mm	0.1 mm	0.1 mm	0.05 mm	0.13 mm	0.25 mm	0.13 mm	
	[0.00197 in]	[0.0039 in]	[0.0039 in]	[0.00197 in]	[0.00512 in]	[0.00984 in]	[0.00512 in]	
31-50	0.1 mm	0.6 mm	0.6 mm	0.13 mm	0.13 mm	0.4 mm	0.13 mm	
	[0.0039 in]	[0.024 in]	[0.024 in]	[0.00512 in]	[0.00512 in]	[0.016 in]	[0.00512 in]	
51-100	0.1 mm	0.6 mm	1.5 mm	0.13 mm	0.13 mm	0.5 mm	0.13 mm	
	[0.0039 in]	[0.024 in]	[0.0591 in]	[0.00512 in]	[0.00512 in]	[0.020 in]	[0.00512 in]	
101-150	0.2 mm	0.6 mm	3.2 mm	0.4 mm	0.4 mm	0.8 mm	0.4 mm	
	[0.0079 in]	[0.024 in]	[0.126 in]	[0.016 in]	[0.016 in]	[0.031 in]	[0.016 in]	
151-170	0.2 mm	1.25 mm	3.2 mm	0.4 mm	0.4 mm	0.8 mm	0.4 mm	
	[0.0079 in]	[0.0492 in]	[0.126 in]	[0.016 in]	[0.016 in]	[0.031 in]	[0.016 in]	
171-250	0.2 mm	1.25 mm	6.4 mm	0.4 mm	0.4 mm	0.8 mm	0.4 mm	
	[0.0079 in]	[0.0492 in]	[0.252 in]	[0.016 in]	[0.016 in]	[0.031 in]	[0.016 in]	
251-300	0.2 mm	1.25 mm	12.5 mm	0.4 mm	0.4 mm	0.8 mm	0.8 mm	
	[0.0079 in]	[0.0492 in]	[0.4921 in]	[0.016 in]	[0.016 in]	[0.031 in]	[0.031 in]	
301-500	0.25 mm	2.5 mm	12.5 mm	0.8 mm	0.8 mm	1.5 mm	0.8 mm	
	[0.00984 in]	[0.0984 in]	[0.4921 in]	[0.031 in]	[0.031 in]	[0.0591 in]	[0.031 in]	
> 500 See para. 6.3 for calc.	0.0025 mm /volt	0.005 mm /volt	0.025 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt	

B1 - Internal Conductors

B2 - External Conductors, uncoated, sea level to 3050 m [10,007 feet]

B3 - External Conductors, uncoated, over 3050 m [10,007 feet]

B4 - External Conductors, with permanent polymer coating (any elevation)

A5 - External Conductors, with conformal coating over assembly (any elevation)

A6 - External Component lead/termination, uncoated, sea level to 3050 m [10,007 feet]

A7 - External Component lead termination, with conformal coating (any elevation)

# Appendix E Visual Comparisons of SnPb and Lead Free Solder Connections

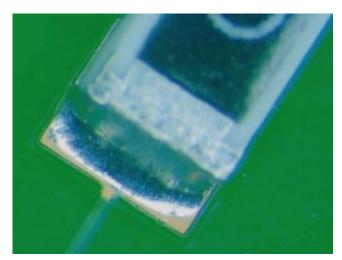


Figure E-1 SnPb Solder; No Clean Process

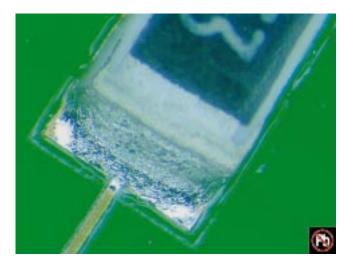


Figure E-2 SnAgCu Solder; No Clean Process

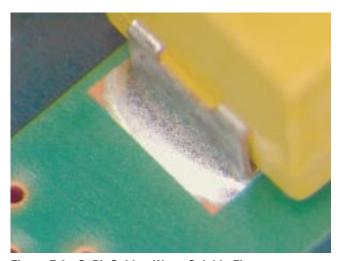


Figure E-3 SnPb Solder; Water Soluble Flux

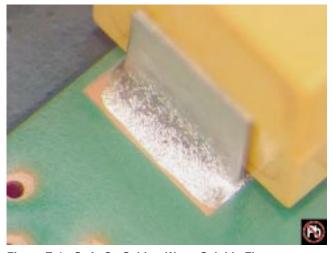


Figure E-4 SnAgCu Solder; Water Soluble Flux

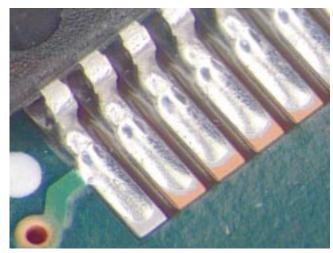


Figure E-5 SnPb Solder; Water Soluble Flux

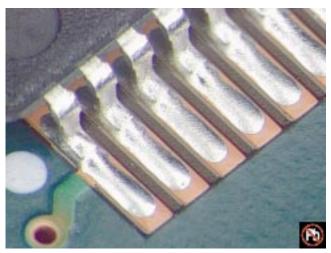


Figure E-6 SnAgCu Solder; Water Soluble Flux

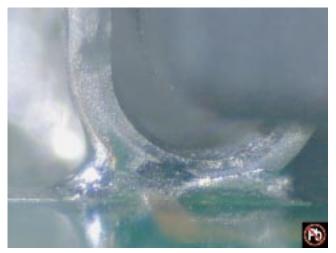


Figure E-7 SnAgCu Solder; No Clean Process, N2 Reflow



Figure E-8 SnAgCu Solder, No Clean Process; Air Reflow



Figure E-9 SnPb Solder; No Clean Process



Figure E-10 SnAgCu Solder; No Clean Process

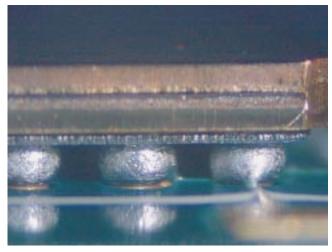


Figure E-11 SnPb Solder; No Clean Process

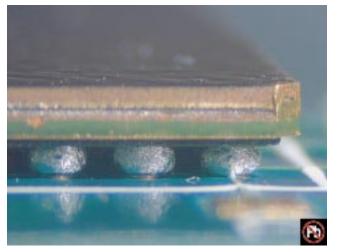


Figure E-12 SnAgCu Solder; No Clean Process

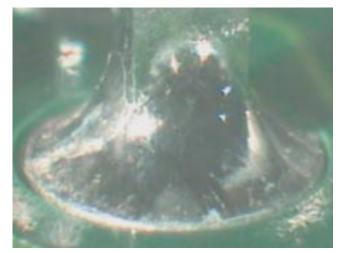


Figure E-13 SnPb Solder



Figure E-14 SnAgCu Solder



Figure E-15 SnPb Solder

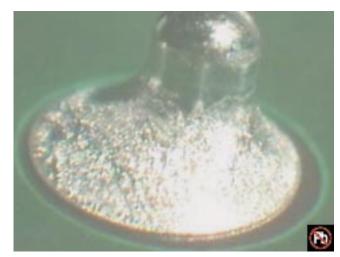


Figure E-16 SnAgCu Solder

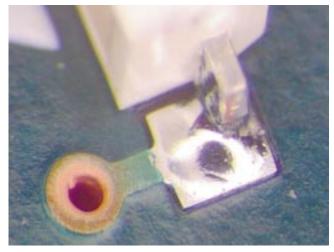


Figure E-17 SnPb Solder; OSP Finish

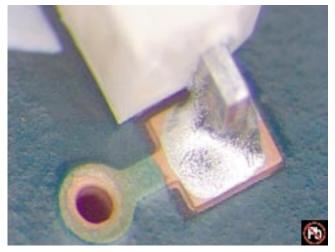


Figure E-18 SnAgCu Solder; OSP Finish



Figure E-19 SnAgCu Solder



Figure E-20 SnAgCu Solder



Figure E-21 SnAgCu Solder



Figure E-22 SnAgCu Solder



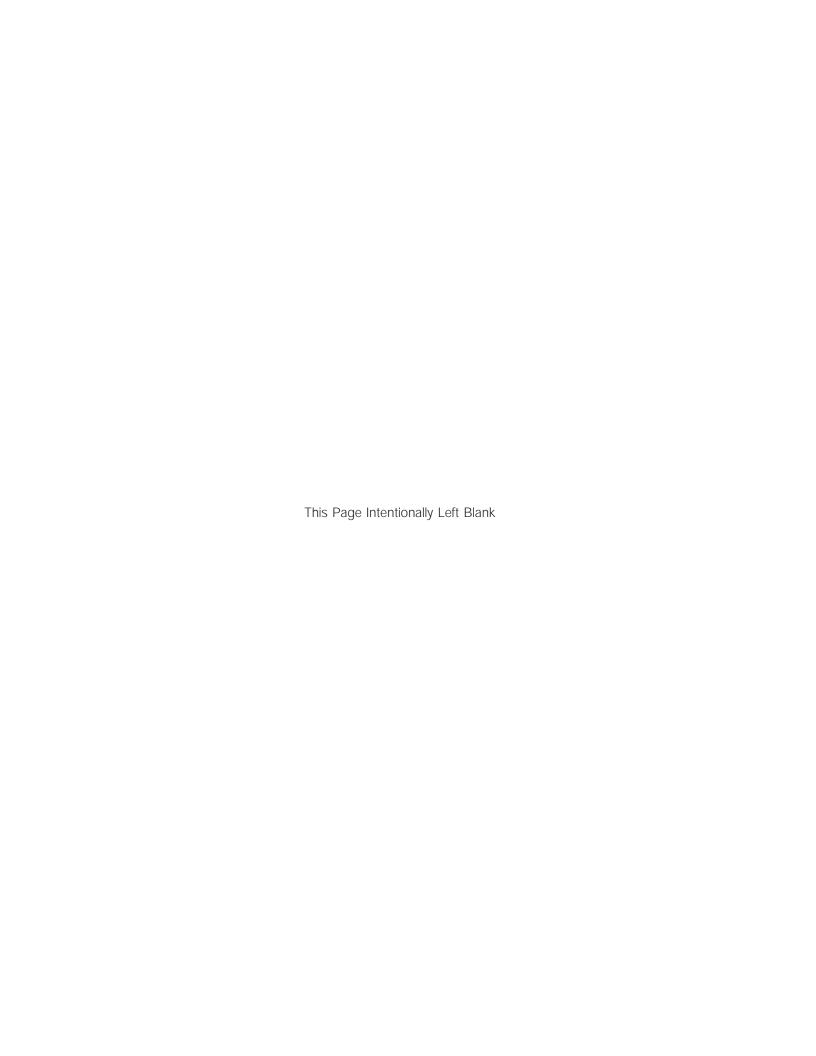
## ANSI/IPC-T-50 Terms and Definitions for **Interconnecting and Packaging Electronic Circuits Definition Submission/Approval Sheet**

The purpose of this form is to keep current with terms routinely used in the industry and their definitions. Individuals or companies are invited to comment. Please

SUBMITTOR INFORMATION:
Name:
Company:
City:
State/Zip:
Telephone:
Date:

complete this form and return	to: C	ity:
PC		tate/Zip:
3000 Lakeside Drive, Suite 30	200	elephone:
Bannockburn, IL 60015-1219 Fax: 847 615.7105		ate:
☐ This is a <b>NEW</b> term and de		
☐ This is a NEW term and de ☐ This is an ADDITION to an ☐ This is a CHANGE to an ex	existing te	rm and definition(s).
Term		Definition
		If space not adequate, use reverse side or attach additional sheet(s)
Artwork: ☐ Not Applicable☐ Included: Electro	•	d 👊 To be supplied ime:
Document(s) to which this terr	m applies:	
	-	
Committees affected by this te	erm:	
		Office Use
IPC O		Committee 2-30
Date Received:		Date of Initial Review:
		Comment Resolution:
Returned for Action:		Committee Action: ☐ Accepted ☐ Rejected
Revision Inclusion:		Accept Modify
		IEC Classification

## Classification Code • Serial Number Terms and Definition Committee Final Approval Authorization: Committee 2-30 has approved the above term for release in the next revision. IPC 2-30 Committee: Date:



## **Technical Questions**

The IPC staff will research your technical question and attempt to find an appropriate specification interpretation or technical response. Please send your technical query to the technical department via:

tel: 847-615-7100 fax: 847-615-7105 www.ipc.org e-mail: answers@ipc.org

## IPC World Wide Web Page www.ipc.org

Our home page provides access to information about upcoming events, publications and videos, membership, and industry activities and services. Visit soon and often.

## **IPC Technical Forums**

IPC technical forums are opportunities to network on the Internet. It's the best way to get the help you need today! Over 2,500 people are already taking advantage of the excellent peer networking available through e-mail forums provided by IPC. Members use them to get timely, relevant answers to their technical questions. Contact KeachSasamori@ipc.org for details. Here are a few of the forums offered.

## TechNet@ipc.org

TechNet forum is for discussion of issues related to printed circuit board design, assembly, manufacturing, comments or questions on IPC specifications, or other technical inquiries. IPC also uses TechNet to announce meetings, important technical issues, surveys, etc.

## ComplianceNet@ipc.org

ComplianceNet forum covers environmental, safety and related regulations or issues.

## DesignersCouncil@ipc.org

Designers Council forum covers information on upcoming IPC Designers Council activities as well as information, comments, and feedback on current designer issues, local chapter meetings, new chapters forming, job opportunities and certification. In addition, IPC can set up a mailing list for your individual Chapter so that your chapter can share information about upcoming meetings, events and issues related specifically to your chapter.

## Trainingnews@ipc.org

This is an announcement forum where subscribers can receive notice of new IPC Training Products.

## leadfree.ipc.org

This forum acts as a peer interaction resource for staving on top of lead elimination activities worldwide and within IPC.

### IPC New Releases@ipc.org

This is an announcement forum where subscribers can receive notice of new IPC publications, updates and standards.

## ADMINISTERING YOUR SUBSCRIPTION STATUS:

All commands (such as subscribe and signoff) must be sent to listserv@ipc.org. Please DO NOT send any command to the mail list address, (i.e.<mail list>@ipc.org), as it would be distributed to all the subscribers.

Example for subscribing: Example for signing off: To: LISTSERV@IPC.ORG To: LISTSERV@IPC.ORG

Subject: Subject:

Message: subscribe TechNet Joseph H. Smith Message: signoff DesignerCouncil

Please note you must send messages to the mail list address ONLY from the e-mail address to which you want to apply changes. In other words, if you want to sign off the mail list, you must send the signoff command from the address that you want removed from the mail list. Many participants find it helpful to signoff a list when travelling or on vacation and to resubscribe when back in the office.

### How to post to a forum:

To send a message to all the people currently subscribed to the list, just send to <mail list>@ipc.org. Please note, use the mail list address that you want to reach in place of the <mail list> string in the above instructions.

Example:

To: TechNet@IPC.ORG Subject: <your subject> Message: <your message>

The associated e-mail message text will be distributed to everyone on the list, including the sender. Further information on how to access previous messages sent to the forums will be provided upon subscribing.

For more information, contact Keach Sasamori tel: 847-597-2815 fax: 847-615-5615 e-mail: sasako@ipc.org www.ipc.org/emailforums

## **Education and Training**

IPC conducts local educational workshops and national conferences to help you better understand conventional and emerging technologies. Members receive discounts on registration fees. Visit www.ipc.org to see what programs are coming to your area.

## **IPC Certification Programs**

IPC provides world-class training and certification programs based on several widely-used IPC standards, including IPC-A-600, IPC-A-610, IPC/WHMA-A-620, J-STD-001 and IPC-7711A/7721A Rework and Repair. IPC-sponsored certification gives your company a competitive advantage and your workforce valuable recognition.

For more information on these programs:

tel: 847-597-2814 fax: 847-615-7105 e-mail: certification@ipc.org www.ipc.org/certification

## Designer Certification (C.I.D.)/Advanced Designer Certification (C.I.D.+)

Contact:

tel: 847-597-2827 fax: 847-615-5627 e-mail: christipoulsen@ipc.org http://dc.ipc.org

## **EMS Program Manager Certification**

Contact:

tel: 847-597-2884 fax: 847-615-5684 e-mail: susanfilz@ipc.org www.ipc.org/certification

## **IPC Video Tapes and CD-ROMs**

IPC video tapes and CD-ROMs can increase your industry know-how and on the job effectiveness. Members receive discounts on purchases.

For more information on IPC Video/CD Training, contact Mark Pritchard

tel: 505/758-7937 ext. 202 fax: 505/758-7938 e-mail: markp@ipcvideo.org http://training.ipc.org

## IPC Printed Circuits Expo, APEX and the Designers Summit



This yearly event is the largest electronics interconnection event in North America. With technical paper presentations, educational courses, standards development meetings networking opportunities and designers certification, there's something for everyone in the industry. The premier technical conference draws experts from around the globe. 500 exhibitors and 6,000 attendees typically

participate each year. You'll see the latest in technologies, products and services and hear about the trends that affect us all. Go to www.GoIPCShows.org or contact shows@ipc.org for more information.

### **Exhibitor information:**

Mary Mac Kinnon Alicia Balonek

Director, Show Sales Director, Trade Show Operations

847-597-2886 847-597-2898

MaryMacKinnon@ip c.org AliciaBalonek@ipc.org

## How to Get Involved

The first step is to join IPC. An application for membership can be found in the back of this publication. Once you become a member, the opportunities to enhance your competitiveness are vast. Join a technical committee and learn from our industry's best while you help develop the standards for our industry. Participate in market research programs which forecast the future of our industry. Participate in Capitol Hill Day and lobby your Congressmen and Senators for better industry support. Pick from a wide variety of educational opportunities: workshops, tutorials, and conferences. More up-to-date details on IPC opportunities can be found on our web page: www.ipc.org.

For information on how to get involved, contact:

Jeanette Ferdman, Membership Director

tel: 847-597-2809 fax: 847-597-7105 e-mail: JeanetteFerdman@ipc.org www.ipc.org



Thank you for your decision to join IPC, Association Connecting Electronics Industries. IPC membership is site specific, which means that benefits of IPC membership are extended only to employees at the site that is designated on this application.

To help IPC serve your member site in the most effective manner possible, please tell us what work is being done at your site by choosing the most appropriate member category. (Check one box only.)

INDEPENDENT PRINTED CIRCUIT BOARD MANUE	ACTURER
This facility manufactures, and sells to other companies, printed wiring boards (F products on the merchant market.	PWB's) or other electronic interconnection
What products do you make for sale?	
One- and two-sided rigid, multilayer printed boards Flexible printed boards	ds
Site General Manager	
Name	Title
■ EMSI COMPANY - Independent Electronics Assembly	
This facility assembles printed wiring boards, on a contract basis, and may offer ot	ther electronic interconnection products for sale.
Site General Manager	·
Name	Title
OEM - Original Equipment Manufacturer  This facility purchases and/or manufactures printed wiring boards or other interce which we manufacture and sell.  What is your company's primary product line?	onnection products for use in a final product,
Site General Manager	
Name	Title
■ INDUSTRY SUPPLIER	
This facility supplies raw materials, machinery, equipment, or services used in the interconnection products.	ne manufacture or assembly of electronic
What products or services does your company supply? (50 word limit, please) The information that you provide here will appear in the next edition of the IPC $N$	
Our company supplies:	
GOVERNMENT AGENCY/ACADEMIC TECHNICAL I	JAISON

This government agency or accredited university, college or technical training school is directly concerned with design, research and utilization of electronic interconnection devices. (Must be a non-profit or not-for-profit organization.)



Site Information: (Please print o	r type)			
Company Name				
Street Address				
City		State	Zip/Postal Code	Country
Main Switchboard Phone No		Main Fax No.		
Company E-Mail Address		Website URL		
Name of Primary Contact for all IPC ma	tters	Title	Mail Stop	
Phone No.		Fax No	E-Mail	
Name of Senior Management Contact:		Title:	Mail Stop	
Phone No		Fax No	E-Mail	
	Please attach busines	s card of primary contact h	ere.	
Please designate your site's	Technical Representatives:			
For PWB/PWA design-related in	nformation and activities:			
Contact Name	Title	Phone	Fov	E-mail
		Priorie	Fax	E-maii
For PCB fabrication-related info	rmation and activities:			
Contact Name	Title	Phone	Fax	E-mail
For Electronics Assembly-relate	ed information and activities:			
Contact Name	Title	Phone	Fax	E-mail
Please designate your site's l	Management Representativ	res:		
For PWB/PWA design-related in	nformation and activities:			
Contact Name	Title	Phone	Fax	E-mail
For PCB fabrication-related info	rmation and activities:			
Contact Name	Title	Phone	Fax	E-mail
For Electronics Assembly-relate		FIIONE	Гах	⊑-mall
Contact Name	Title	Phone	Fax	E-mail



Ml	EMBERSHIP DUES SCHEDULE	
Ple	<b>\$1,000.00</b> – Annual dues for Primary Site Membership Twelve months of IPC membership begins from the time the application and payment are received at the IPC office.	<ul> <li>TMRC MEMBERSHIP</li> <li>Please send information on participation in the Technology Market Research Council (TMRC) program.</li> <li>Only current IPC member sites are eligible to participate in this calendar year program, which is available for an</li> </ul>
	\$800.00 – Annual dues for Additional Facility Membership An additional membership for a site within an organization where there already is a current Primary Site IPC membership. \$600.00** – Annual dues for an independent PCB/PWA	additional fee.  Yes, sign up our site now:  \$950.00 - Primary TMRC member site  \$400.00 - Additional facility TMRC member. Another site within our organization is already a TMRC program participant.
	fabricator or independent EMSI provider with annual sales of less than \$1,000,000.00. USD ** Please provide proof of annual sales.	Name of Primary Contact for all TMRC matters:
	<b>\$250.00</b> – Annual dues for Government Agency or Academic Technical Liaison Membership. Must be not-for-profit organization.	Phone Fax
		E-Mail
Enc	YMENT INFORMATION  closed is our check/money order for \$	
Fax	or mail application with credit card payment to: IPC *3000 Lakeside Drive, Suite 309S Bannockburn, IL. 60015-1249 Tel: 847-615-7100 Fax: 847-615-7105 * Overnight deliveries to this address only	
Ple	ase bill my credit card (circle one) for \$	
□ N	MasterCard    American Express    Visa    Dir	ners Club
Acco	ount No Expiration Date	
	e of Card Holder	
	orized Signature	
Phor	ne Number	

## **QUESTIONS?**

Call the IPC Member Services Department in Bannockburn, Illinois, at 847-597-2809 or 847-597-2872, or fax us at 847-615-7105.



## INFORMATION DISTRIBUTION

IPC has significant member benefits available to a wide range of individuals within your organization. To ensure that your facility takes advantage of these benefits, please provide the name of the individual responsible for each of the functional areas listed below. If one person has multiple responsibilities, please list that person's name as many times as necessary.

Chief Executive:

Name Sales/Marketing:	Title/Mail Stop	Phone	Fax	E-mail
Name Finance (CFO)	Title/Mail Stop	Phone	Fax	E-mail
Name Human Resources	Title/Mail Stop	Phone	Fax	E-mail
Name Environmental/Safety	Title/Mail Stop	Phone	Fax	E-mail
Name Design/Artwork	Title/Mail Stop	Phone	Fax	E-mail
Name Product Assurance	Title/Mail Stop	Phone	Fax	E-mail
Name Manufacturing	Title/Mail Stop	Phone	Fax	E-mail
Name Training	Title/Mail Stop	Phone	Fax	E-mail
Name Purchasing	Title/Mail Stop	Phone	Fax	E-mail
Name	Title/Mail Stop	Phone	Fax	E-mail
the names of individuals who	RIPTION LIST  IPC membership is a subscription of would benefit from receiving our finterest. A subscription for the IF	magazine, which provides	information about the in	ndustry,
	Name		Title/Mail Stop	
	Name		Title/Mail Stop	
	Name		Title/Mail Stop	
	Name		Title/Mail Stop	
	Name		Title/Mail Stop	
	Name		Title/Mail Stop	



## **Standard Improvement Form**

## IPC J-STD-001D

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to

submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

IPC 3000 Lakeside Drive, Suite 309S Bannockburn, IL 60015-1219 Fax 847 615.7105

E-mail: answers@ipc.org

1. I recommend changes to the following: \_\_\_\_ Requirement, paragraph number \_\_\_\_\_ \_\_\_\_ Test Method number \_\_\_\_\_\_, paragraph number \_\_\_\_\_ The referenced paragraph number has proven to be: \_\_\_ Unclear \_\_\_ Too Rigid \_\_\_ In Error \_\_\_ Other \_\_\_ 2. Recommendations for correction: 3. Other suggestions for document improvement: Submitted by: Name Telephone E-mail Company Address City/State/Zip Date

